8086 MICROPROCESSOR

UNIT -IV

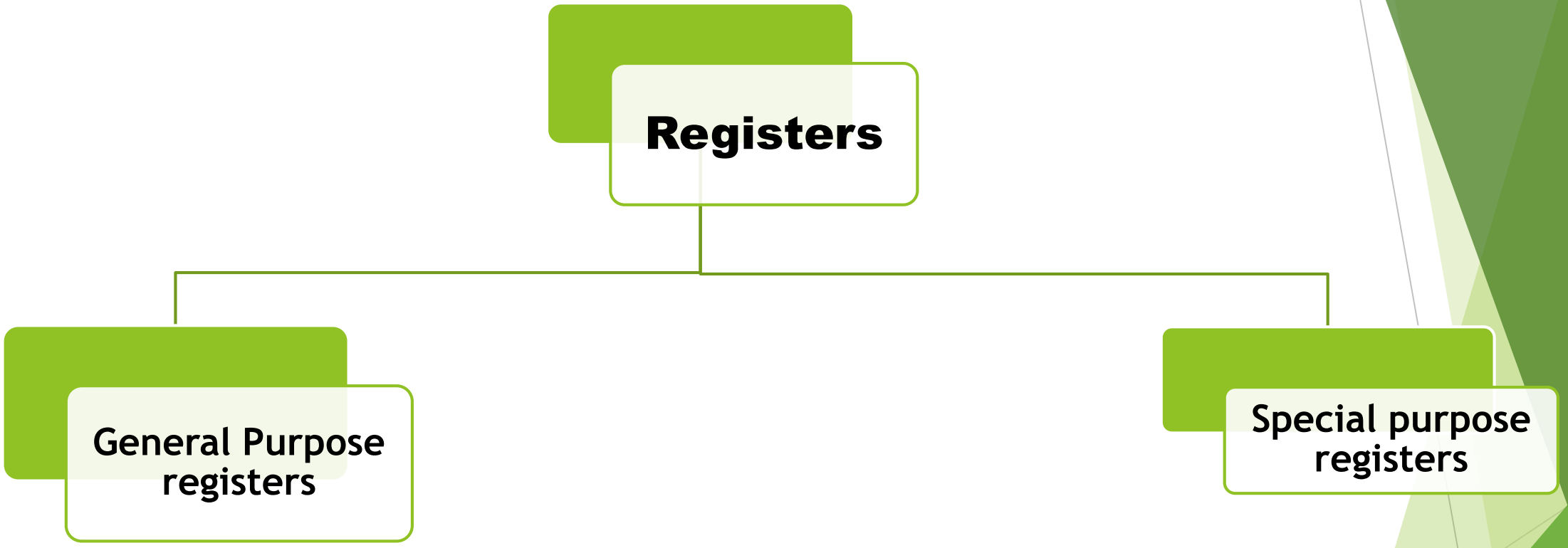
Topics to be covered:

- Architecture of 8086
- Register Organization
- pin description
- Memory Segmentation
- Physical Memory Organization
- Signal descriptions of 8086- Common Function Signals
- Minimum& Maximum mode signals
- Pipelining in 8086 microprocessor.

8086 Microprocessor -Features

- 16 bit
- 40-pin, Dual Inline Packaged IC.
- supports a wide range of instructions-CISC Based
- 20-bit address bus, which can address up to 1 MB of memory
- 16-bit data bus- transfer data between the microprocessor and memory or I/O devices.
- segmented memory architecture- addressed using both a segment register and an offset
- 14 internal registers, each of 16 bits or 2 bytes wide.
- **Main advantage- it supports Pipelining.**

Register Organization

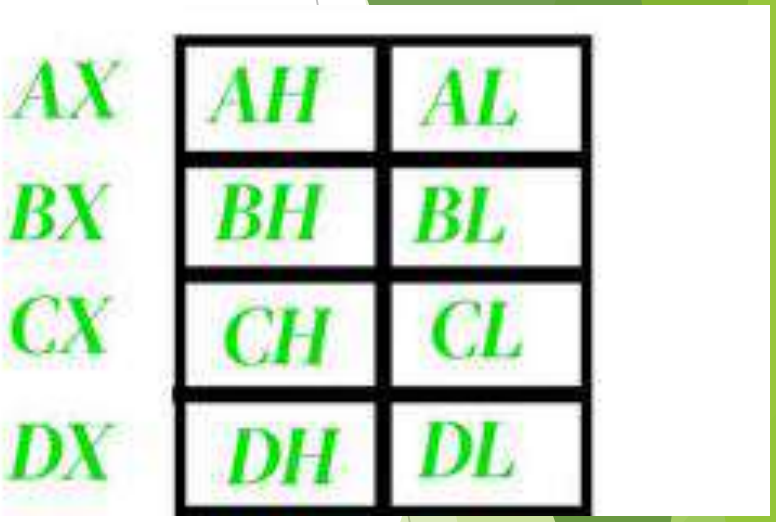


- Holding data
- Variables
- Intermediate results
- Counters
- Offset

- address memory segments
- include the flags register
- instruction pointer (IP)

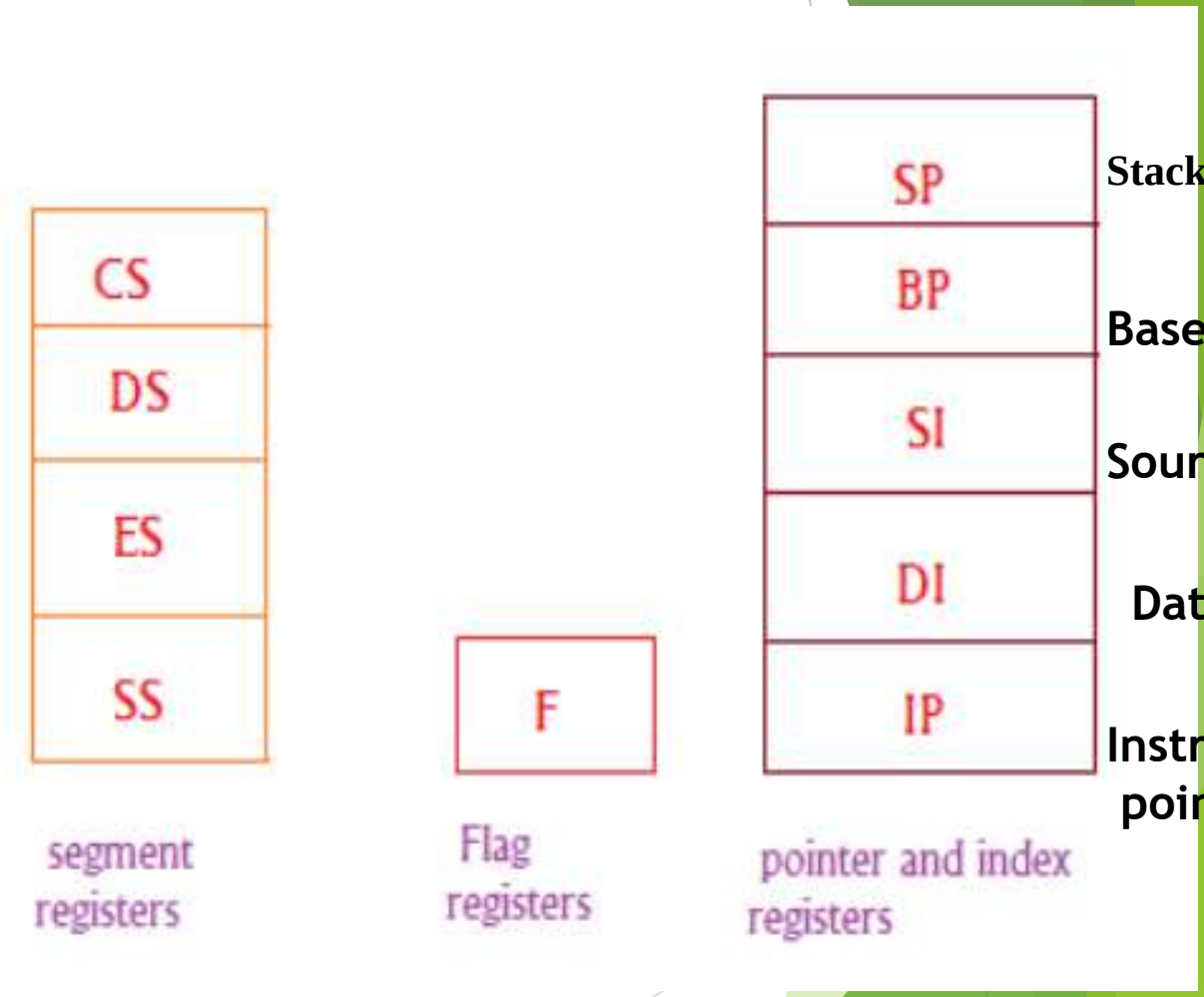
General Purpose Registers

- AX : 16 bit Accumalator
- BX : Used for offset storage for calculating physical address
- CX : Default Counter
- DX : Implicit data or act as destination for certain instructions

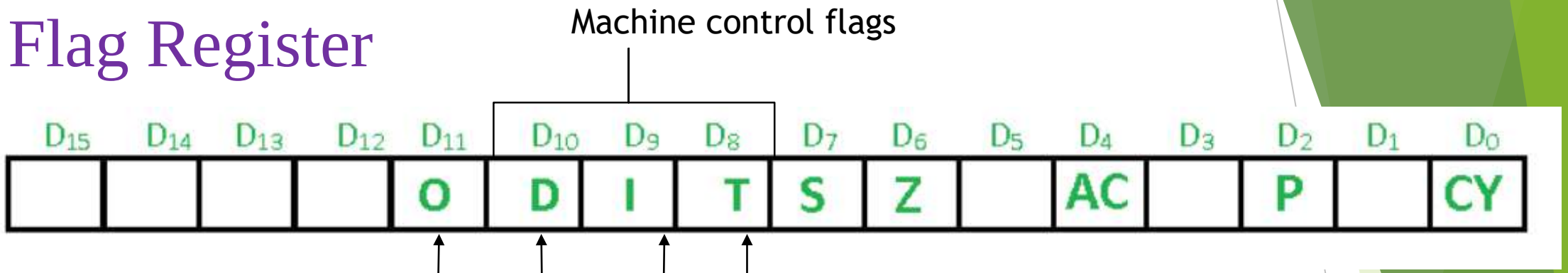


Special Purpose Registers

- Segment registers holds the address of a particular memory segment.
- Flags holds information about the state of the processor after executing an instruction.
- Pointer and Index Registers usually contains offset address



Flag Register



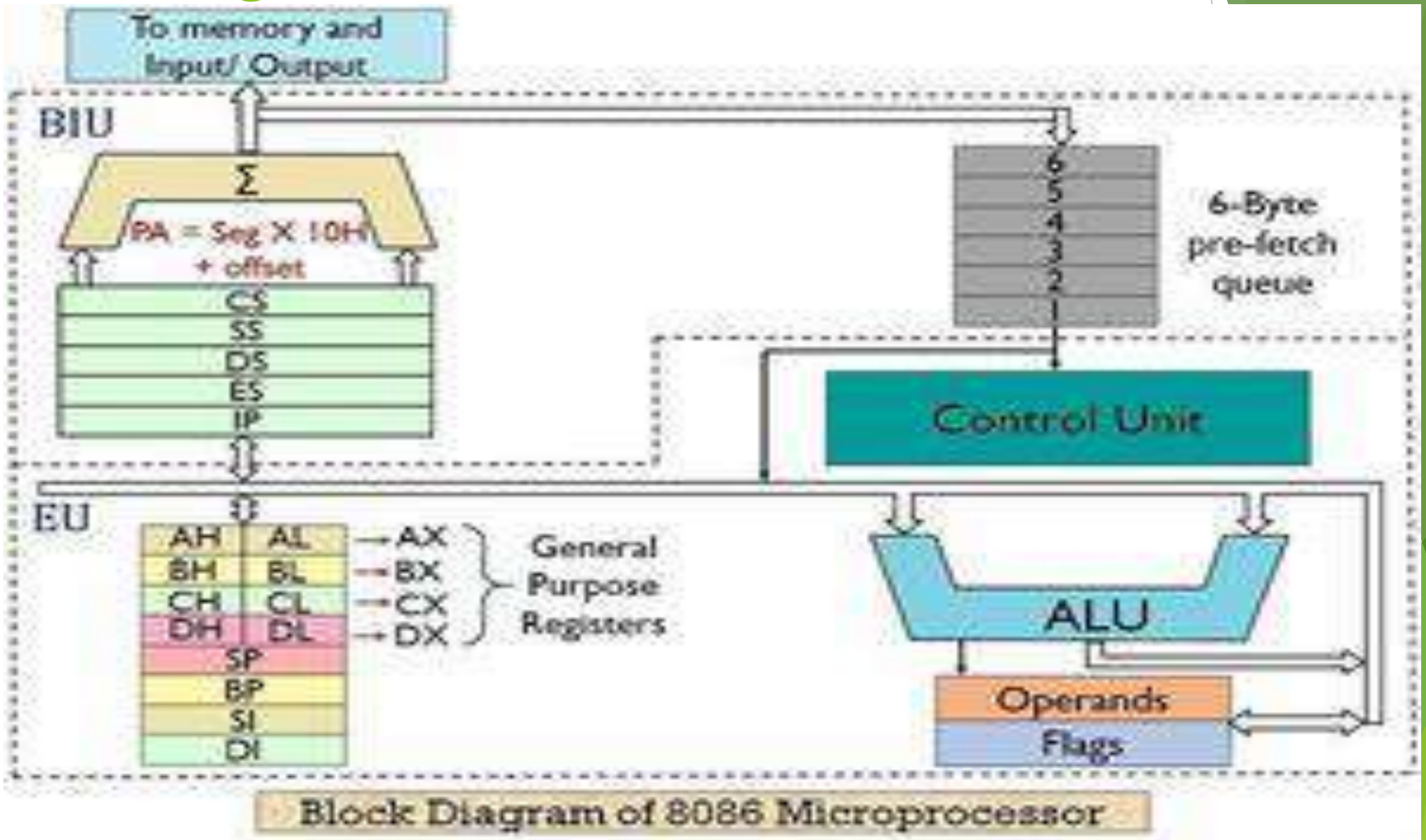
set (1) if the result of a signed operation is too large to fit in the number of bits available to represent it, otherwise reset (0)

flag is specifically used in string instructions. If directional flag is set (1), then access the string data from higher memory location towards lower memory location.

If interrupt flag is set (1), the microprocessor will recognize interrupt requests from the peripherals

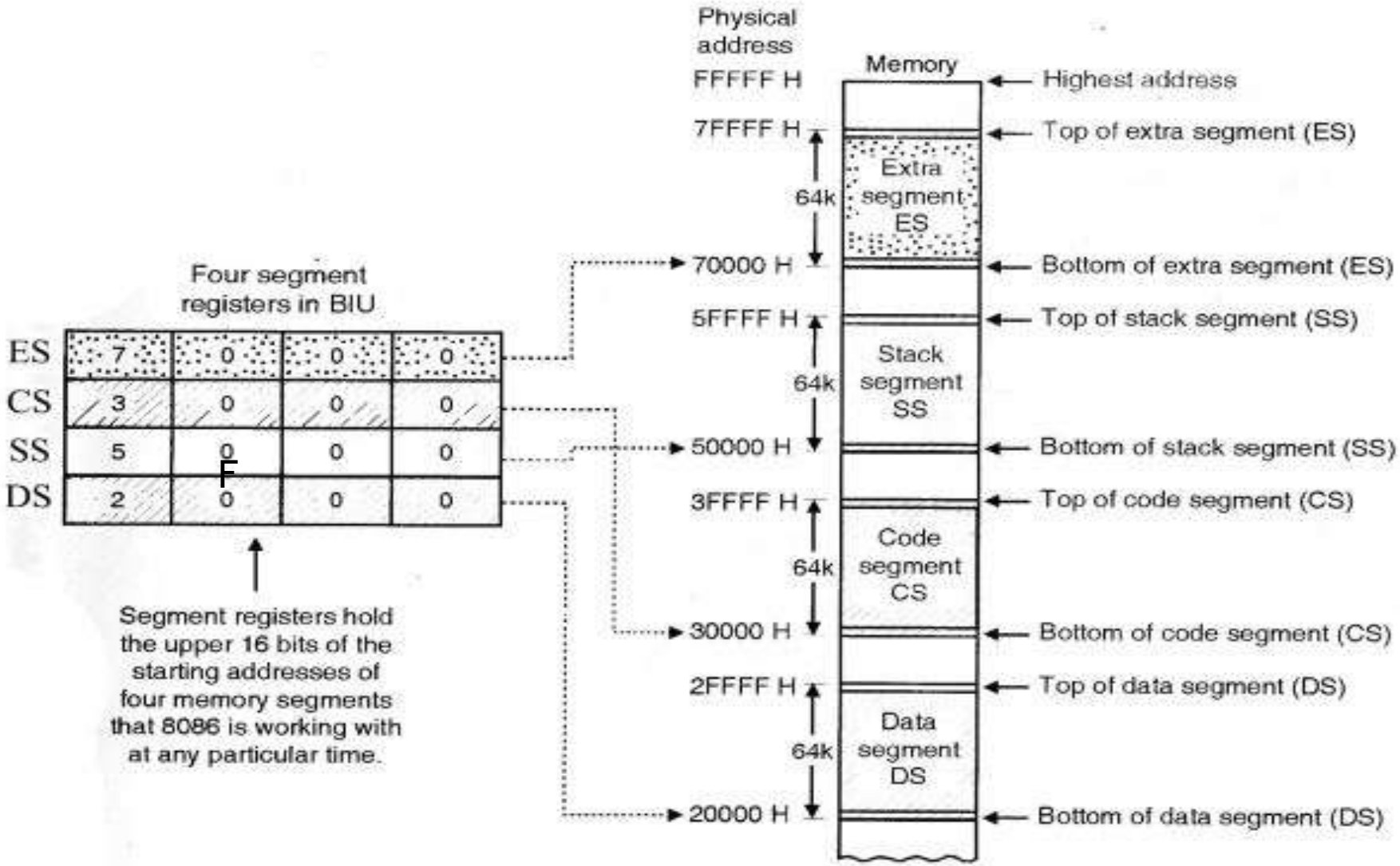
Setting trap flag puts the microprocessor into single step mode for debugging. If trap flag is set (1), the CPU automatically generates an internal interrupt after each instruction,

Block Diagram

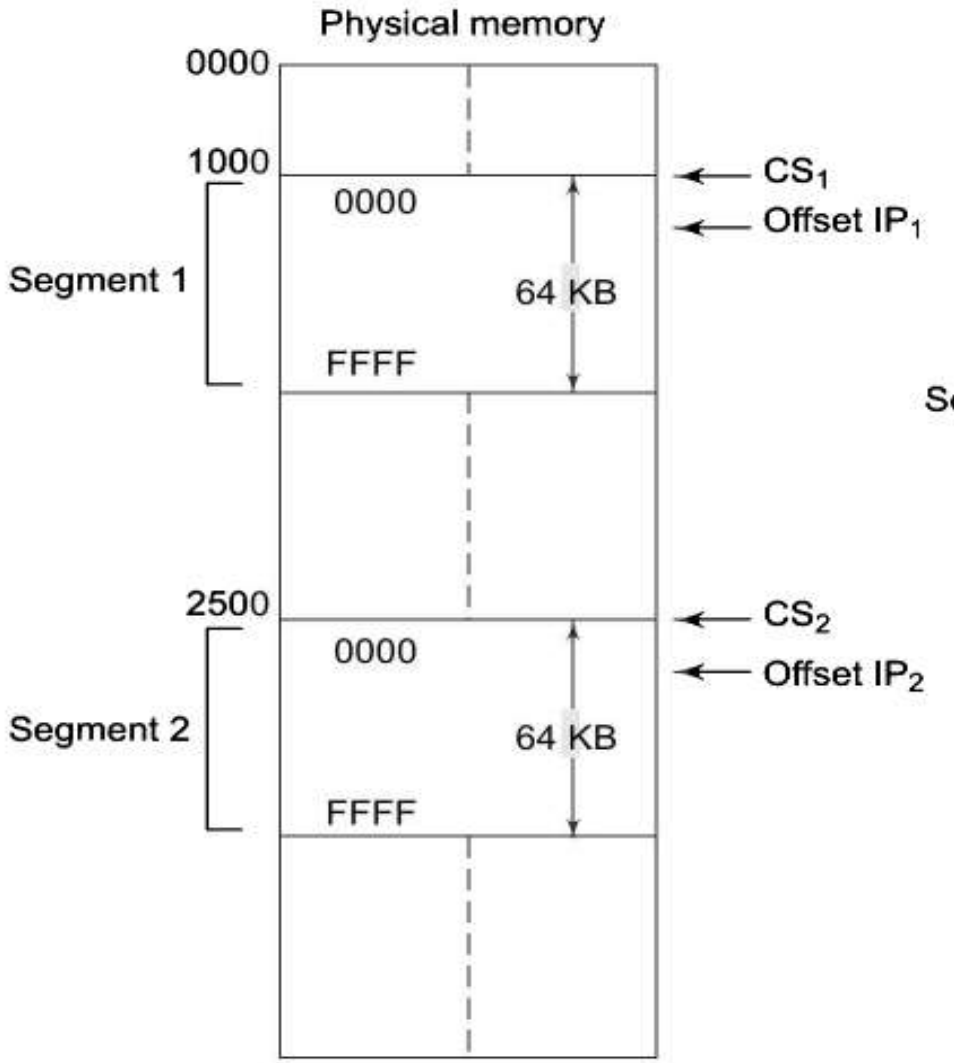


Block Diagram of 8086 Microprocessor

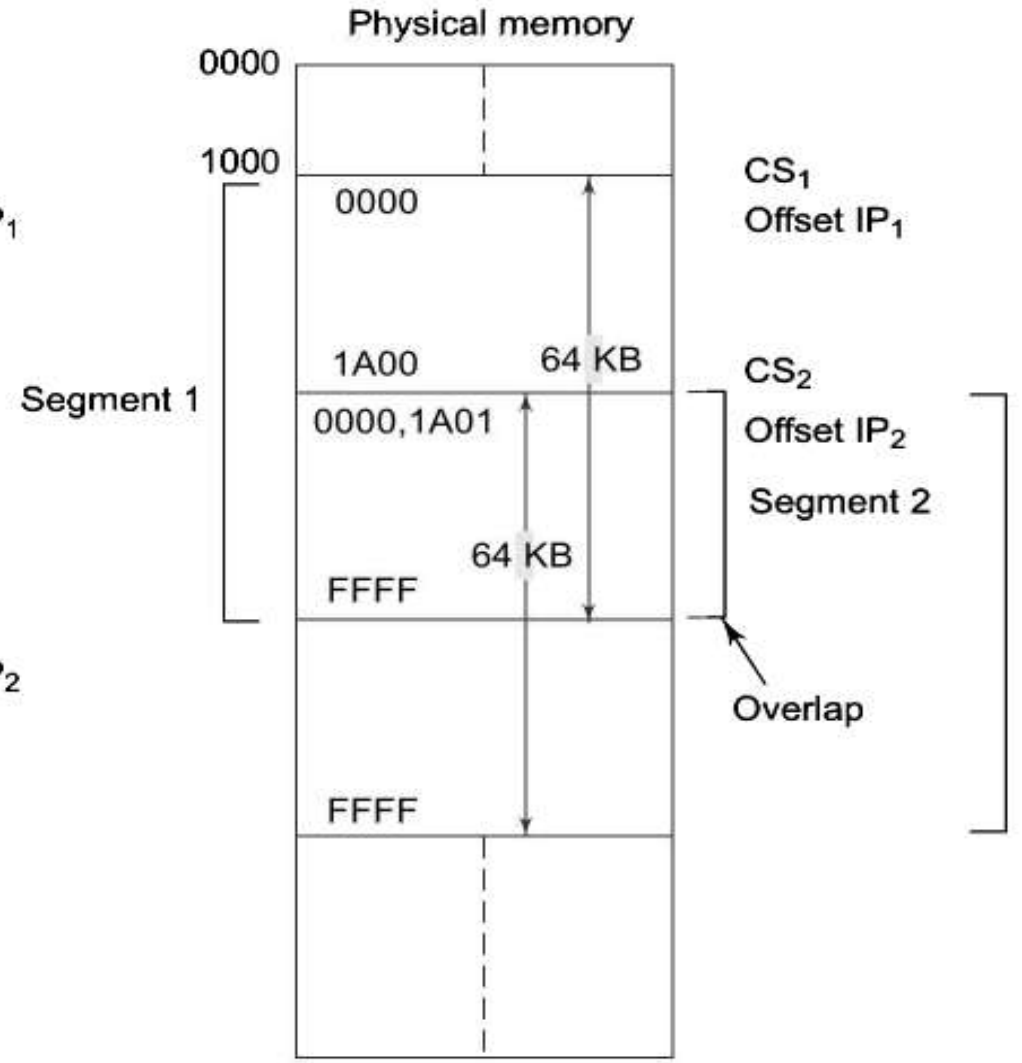
Memory Segmentation



One way of positioning four 64k byte segments within the 1M byte memory space of an 8086



Non overlapping



Overlapping segment

Advantages of segmented memory

- Address handling capacity is 16 bit but can address 1MB memory
- Code, Data and Stack are on different location to avoid overwrite (Data protection)
- Permits program/ its data to be put into different areas of memory

Generating Physical address of Memory

- The 8086 microprocessor can address up to 1 megabyte (MB) of physical memory.
- 1 MB memory is divided into 16 segments, each with a size of 64 KB
- 20-bit physical address by combining the contents of the segment register and the offset register

  Physical address = segment address × 10H + offset address
- The offset address values are from 0000H and FFFFH
- The physical addresses range from 00000H to FFFFFH.

Calculating Physical address

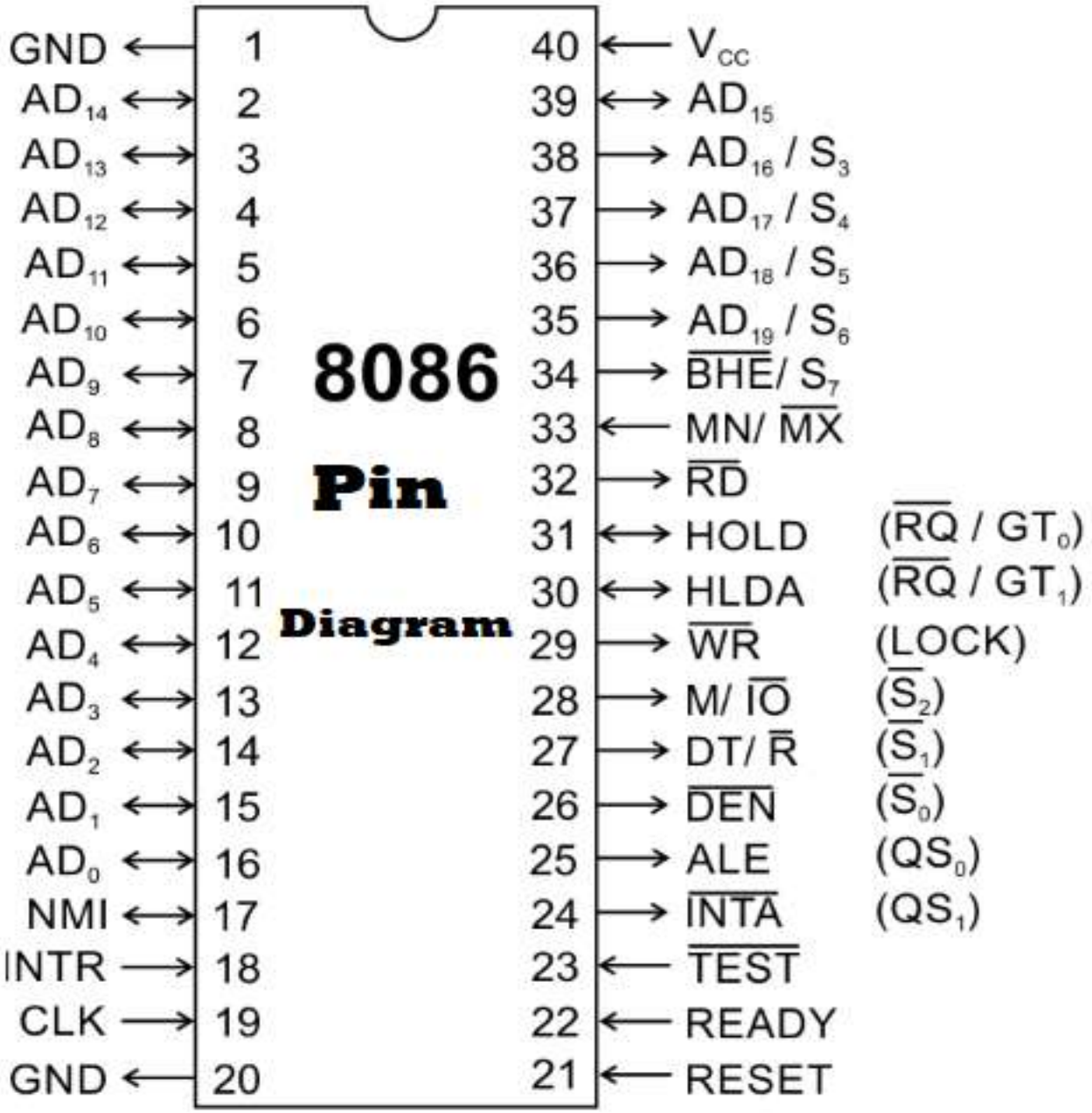
For example, consider the segment address is 2010*H* and the offset address is 3535*H*.

The physical address is calculated as:

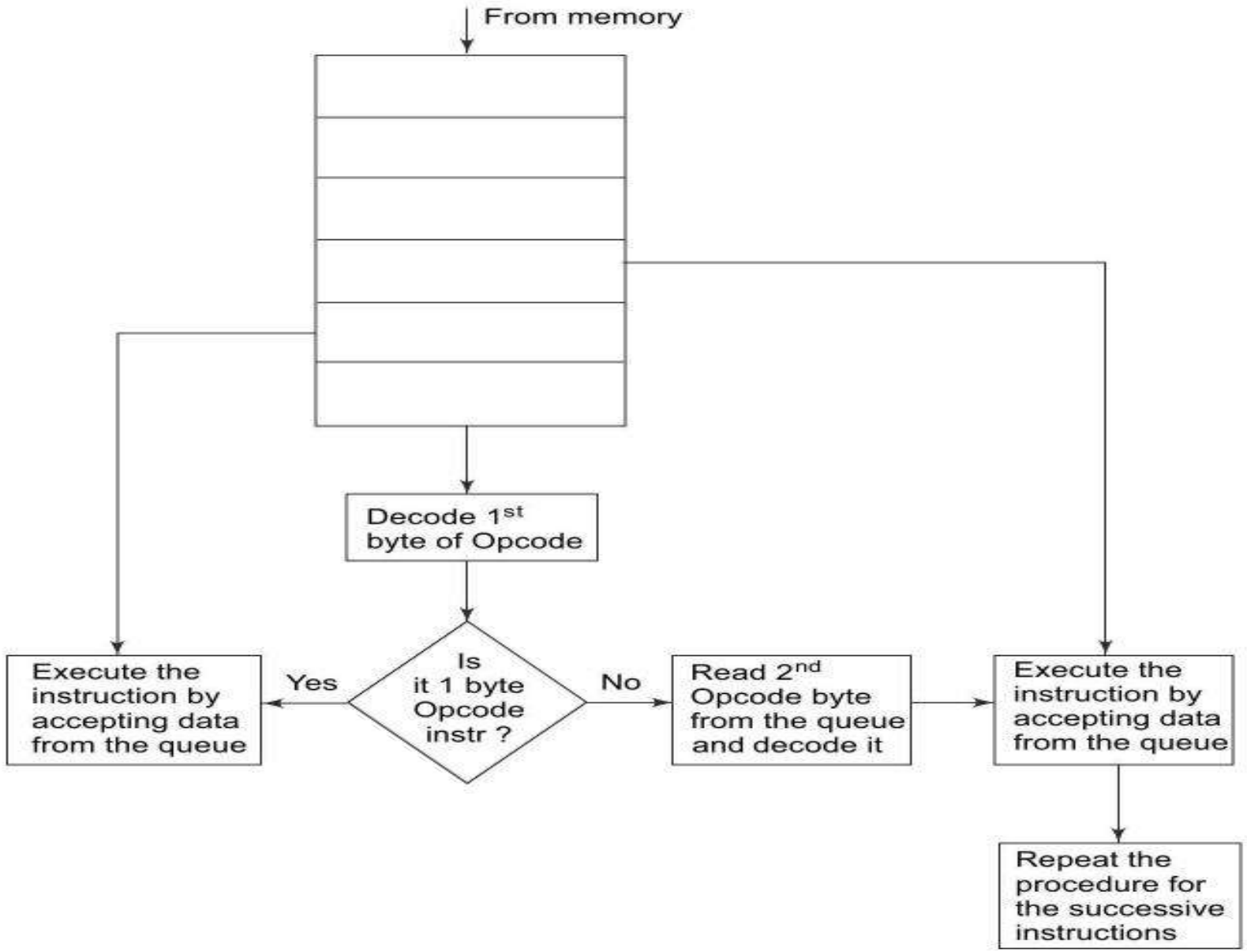
Segment Address	2010*H*		0 0 1 0	0 0 0 0	0 0 0 1	0 0 0 0
Shifted left by 4 bit positions		0 0 1 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0
	+					
offset address			0 0 1 1	0 1 0 1	0 0 1 1	0 1 0 1
physical address		0 0 1 0	0 0 1 1	0 1 1 0	0 0 1 1	0 1 0 1
		2	3	6	3	5

Pin Description

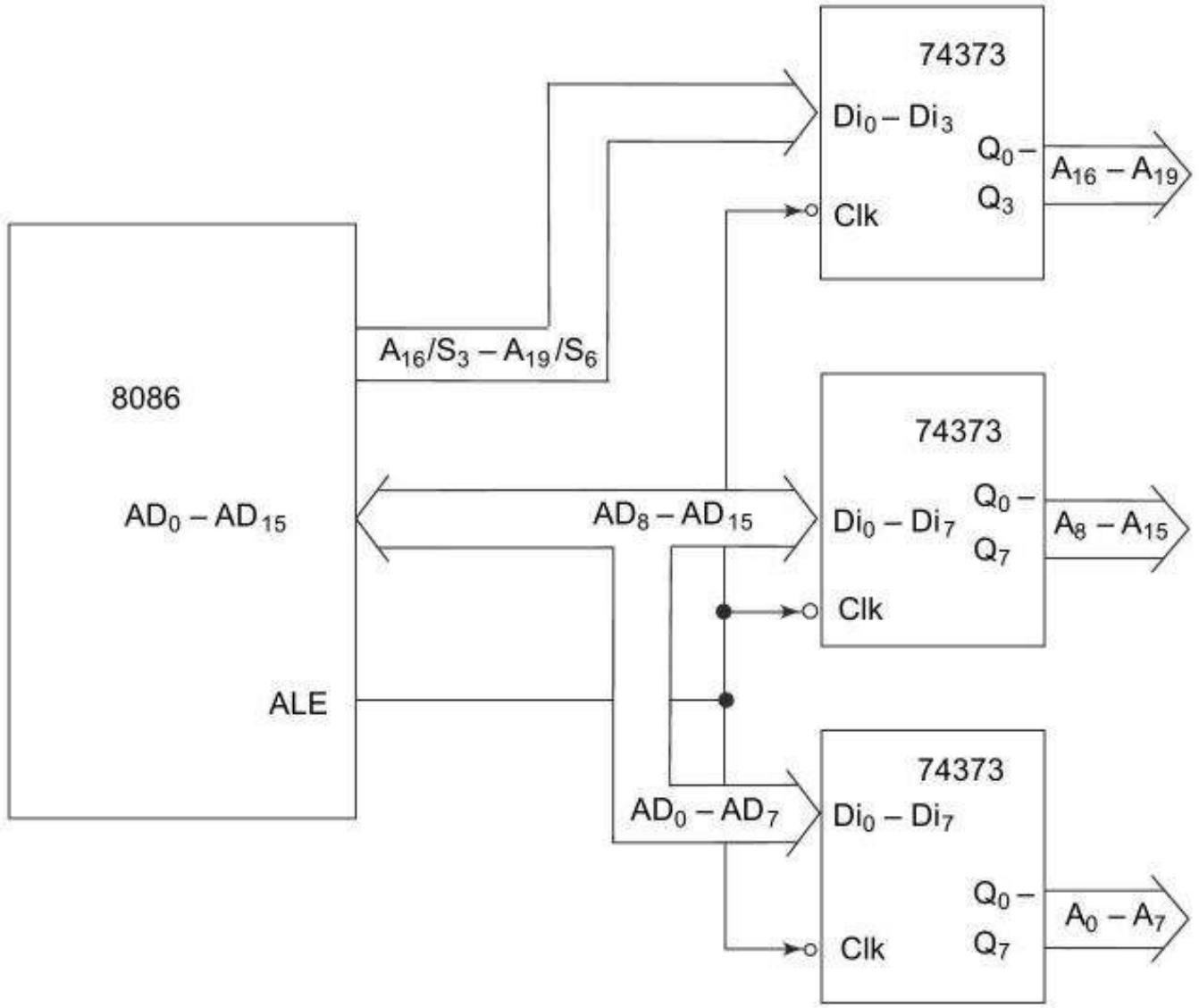
- Pin classification
  - Common Function
  - Only in minimum mode
  - Only in max mode



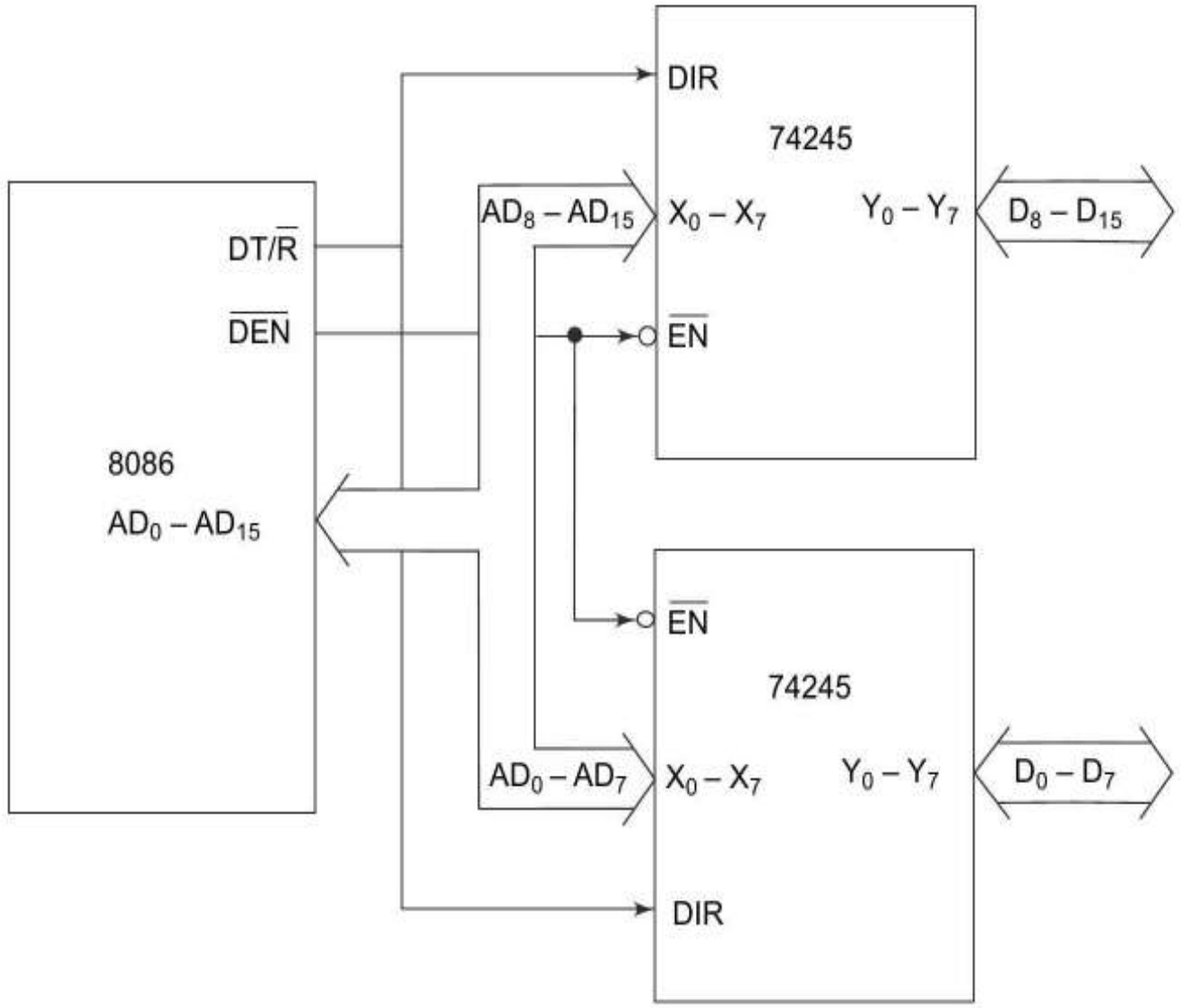
Queue Operation



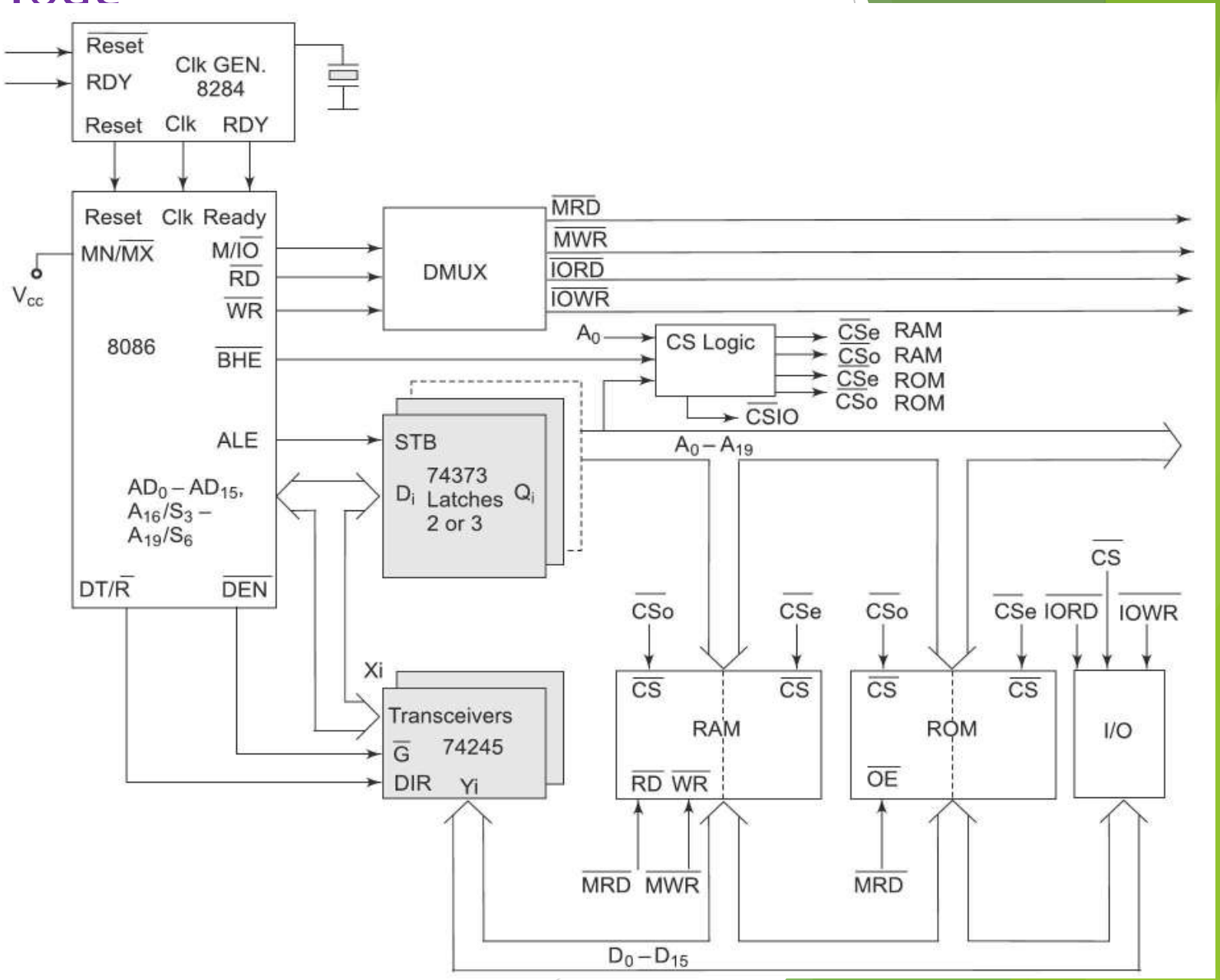
Latching 20 bit address lines



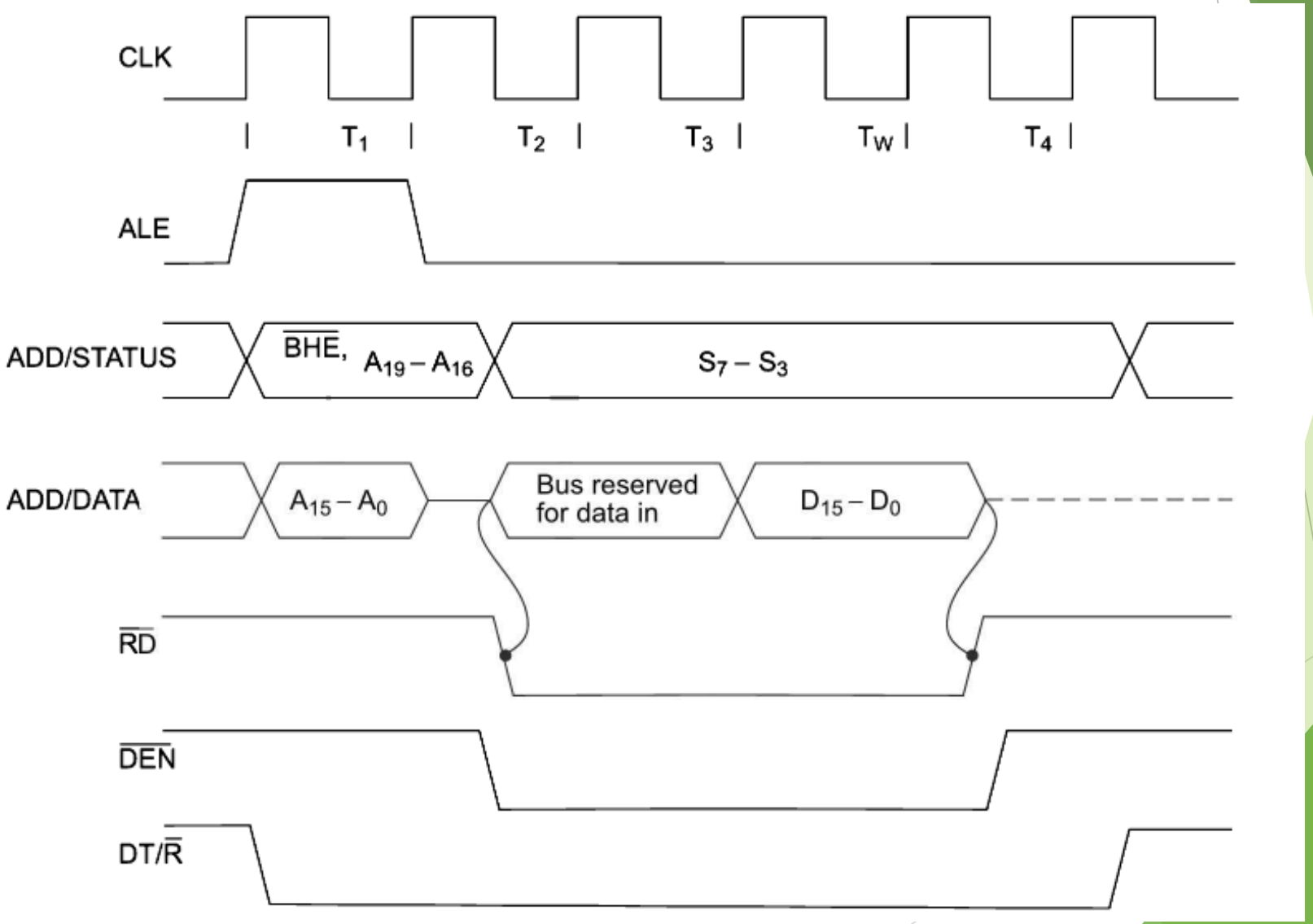
Buffering Data Bus of 8086



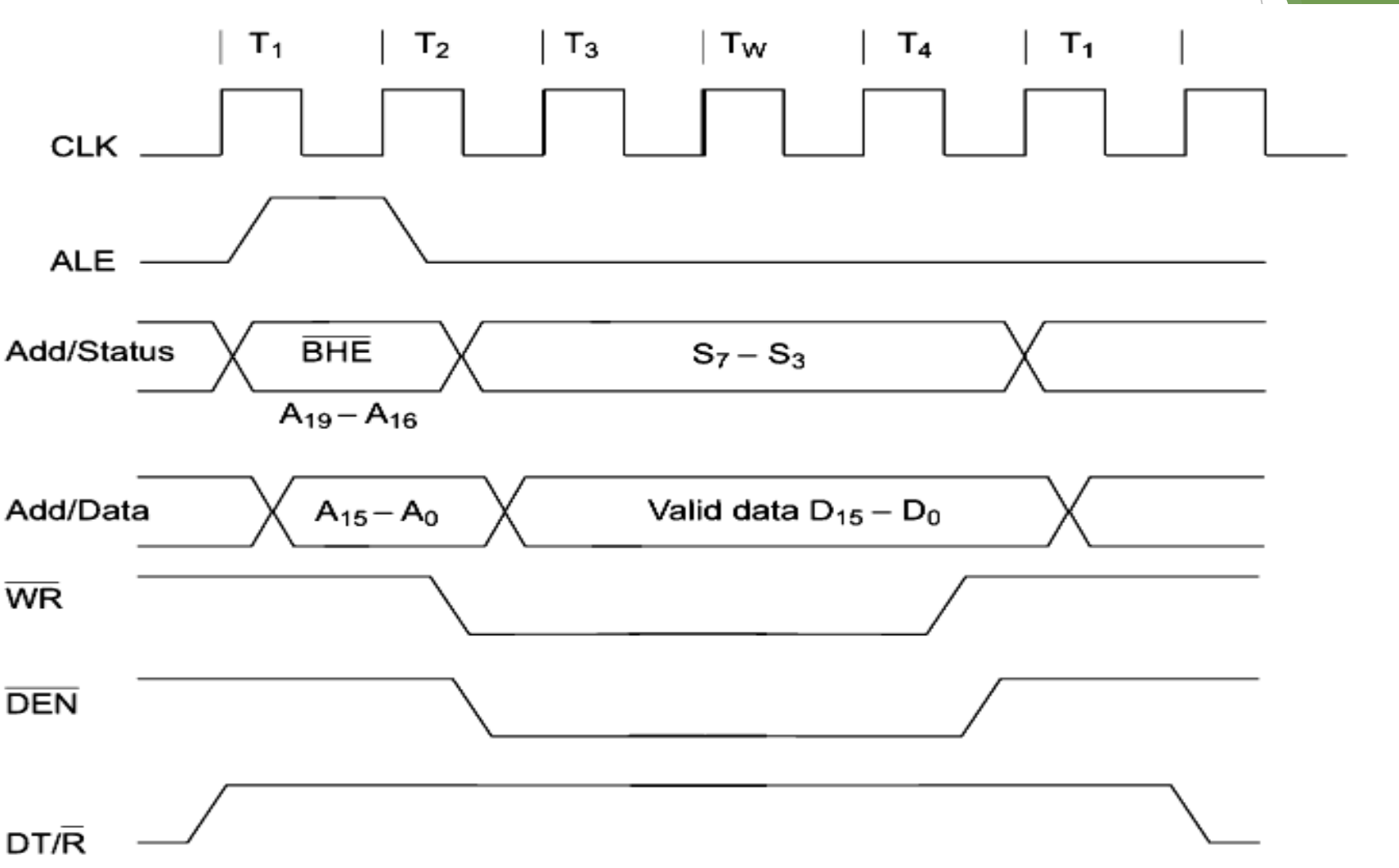
8086 in Minimum Mode



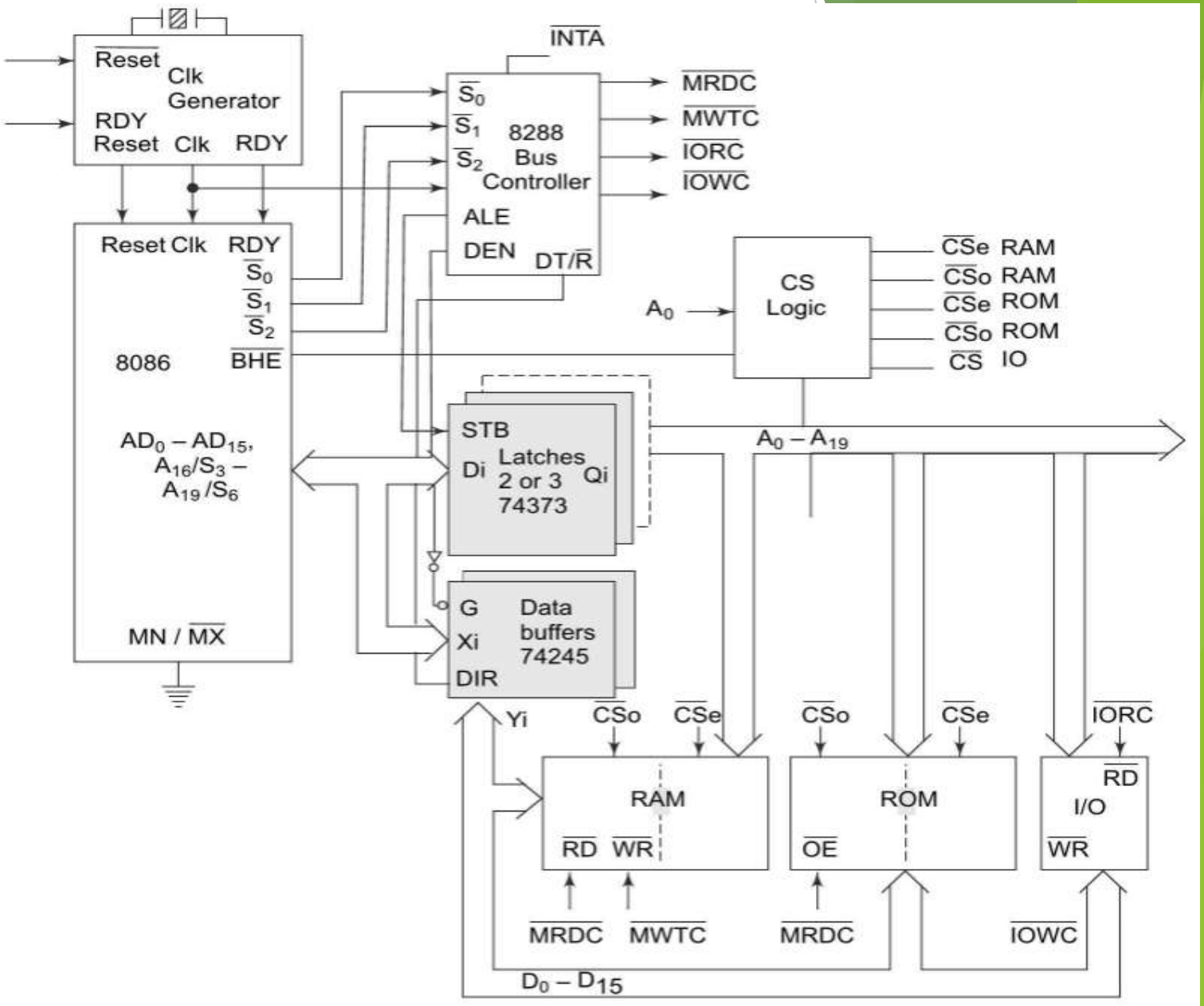
Read cycle in Minimum mode



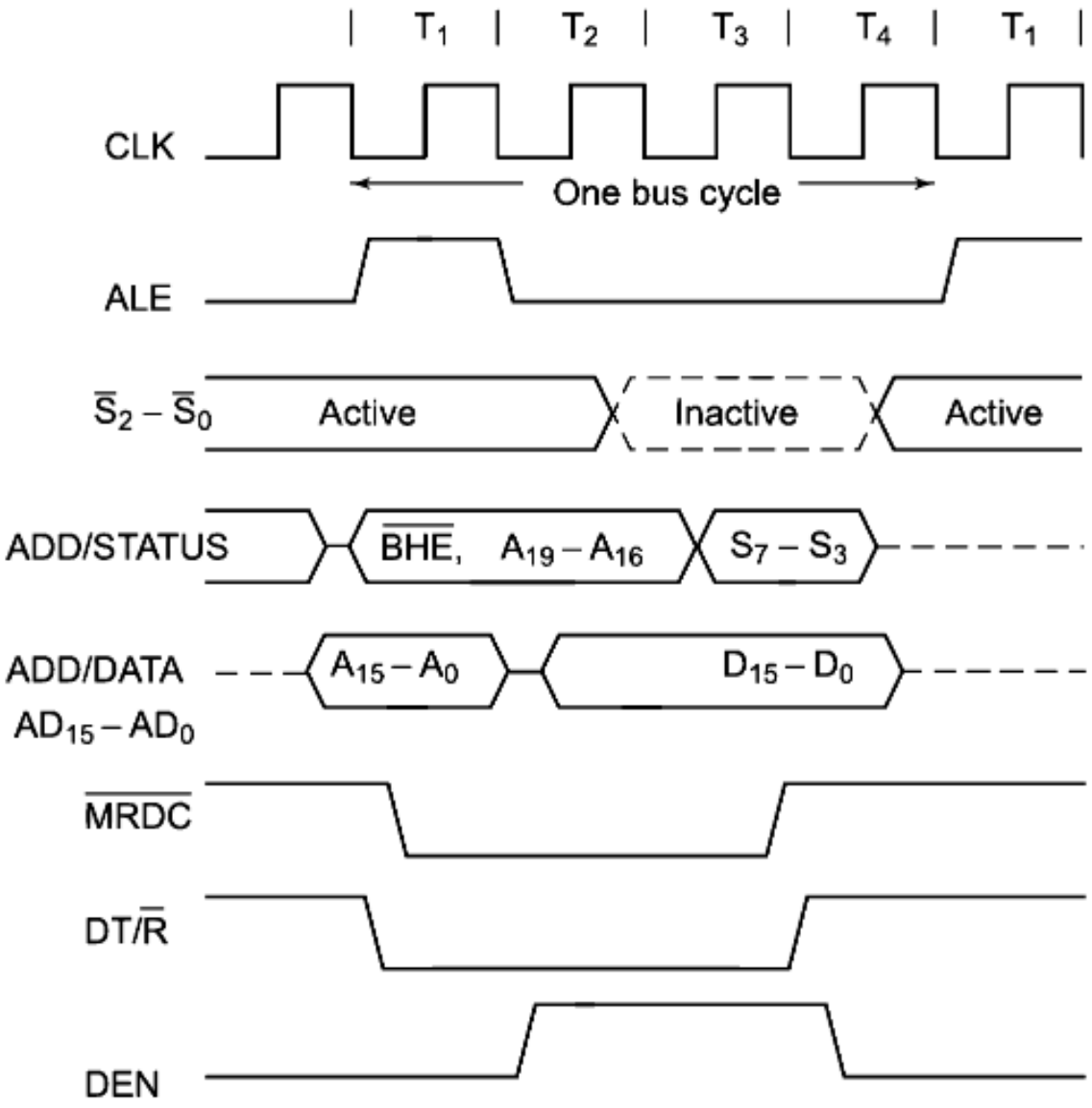
Write cycle in Minimum Mode



Maximum Mode



Read cycle in Maximum Mode



Write cycle in Maximum modes