NOVEL INTEGRATED ELECTRONICS LABS (NINE Labs), IIT Guwahati

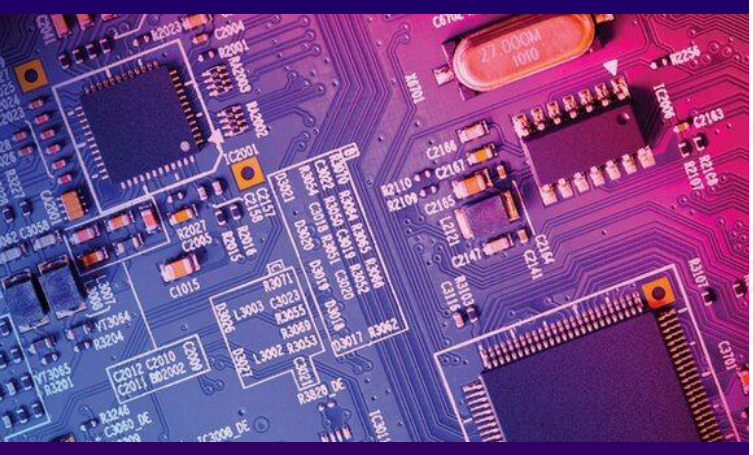
in association with

SGSITS Indore

organising a

One Week Workshop on

"VLSI DESIGN USING OPEN SOURCE TOOLS"



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इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी मंत्रालय
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY
सत्यमेव जयते

23rd-27th February 2026
Spandan Hall, 3rd Floor, ATC Building, SGSITS Indore

OUTCOME

The workshop on Open Source EDA Design tool for VLSI Design, is organized to bring together researchers, developers, and users to discuss advancements, share knowledge, and collaborate on commercial tools for chip design. After completion of this workshop, participants would be able to design analog circuits through VLSI backend flow.

TENTATIVE SPEAKERS

Principal Investigator:
Prof. Gaurav Trivedi
(Professor, Dept. of EEE, IITG)

Keynote Speaker :
Ms. Indira Iyer Almeida
(Program Director, The OpenROAD Init.)

Invited Speakers :
Mr. Gadiparthi Naveen
Mr. Mandapalli Ajay Kumar
Mr. Vijayan Krishnan
(Chipware Team)

DETAILS

Workshop Duration: 1 Week
Last Date to apply: 21st Feb 2026
Workshop Mode: Offline

The participants should carry their own laptop having **min. 08 GB RAM** and **Core i3 Processor [OS: Linux Ubuntu v22]**

Working Lunch will be provided to all participants.
Participants outside Indore have to make their stay arrangements on their own.

OBJECTIVE

The objective of this workshop is typically to impart practical knowledge and skills related to designing, analyzing, and troubleshooting analog electronic circuits. Participants would be able to learn fundamental concepts, circuit topologies and techniques to design circuit from Schematic to GDS-II.

CONTACT US

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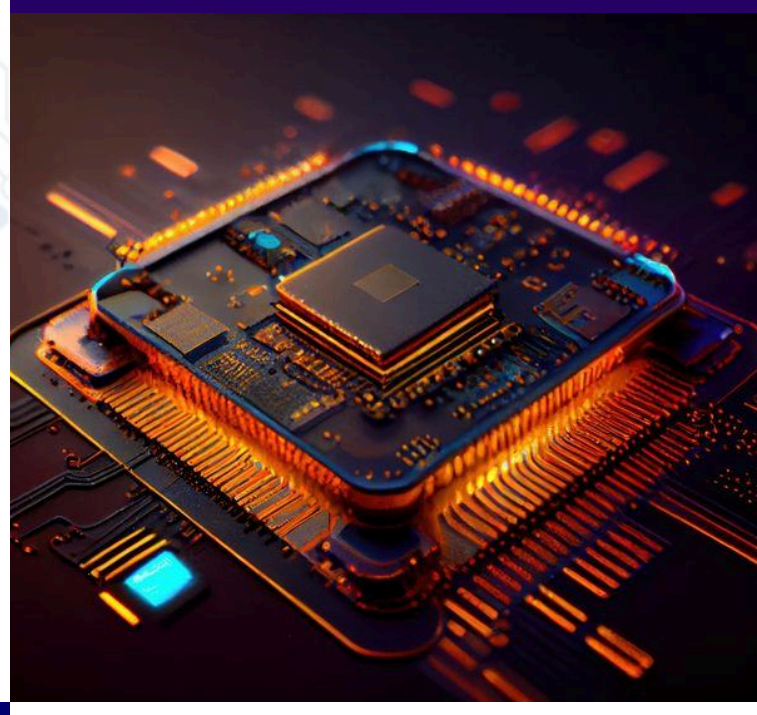

CONTENTS

Introduction to VLSI Backend Flow

- Stages and Sign-off Checks Overview
- OpenROAD Design Flow
- Detailed VLSI Backend Flow
- RTL Synthesis
- Floorplanning
- Placement
- Static Timing Analysis
- Clock Tree Synthesis
- Routing
- GUI OpenROAD for PPA

Hands-on

- Installation of the OpenROAD Tool.
- Input files
- RTL synthesis
- Sanity Checks
- Floorplan and Placement
- Post-placement Timing Analysis
- Clock Tree Synthesis (CTS)
- Post-CTS Timing Analysis
- Routing and DRC/LVS Check

WHO CAN APPLY?

UG/PG students/Research Scholars of EIE/ ECE/EEE/Technical Institutions.

Limited Seats: 50

HOW TO APPLY?

Registration link:

https://forms.gle/VqXfcytnvXqpxxp6A

or

Register via QR code

QR CODE FOR E&I Department Webpage

Patron: Prof. Neetesh Purohit
Director, SGSITS

ORGANIZING COMITTEE

Convenor:	Prof. P.P. Bansod (SGSITS)
Convenor:	Prof. Gaurav Trivedi (IITG)
Co-Convenor:	Dr. R.C. Gurjar, HOD (E&I)
Coordinator:	Dr. Rajesh Khatri (SGSITS)
Co-Coordinator:	Dr. Girish G. Soni
Member:	Mr. D.S. Ajnar
Member:	Dr. Anuj Rawat
Member:	Ms. Tarni Joshi
Member:	Ms. Kirti Bhargawa
Member:	Ms. Disha Sharma
Member:	Dr. Neelesh Jain

TECHNICAL TEAM

Project Associate:	Ms. Mansi Jain
Project Associate:	Ms. Kamini Singh
Lab Assistant:	Mr. A.R. Mansoori
Lab Assistant:	Mr. Gaurav Tomar

VOLUNTEERS

Ajeet Sahani
Shivam Bansal
Priyansh Bharani
Kaushiki Dhoble
Kushwant Kawle
Shakti Gurjar