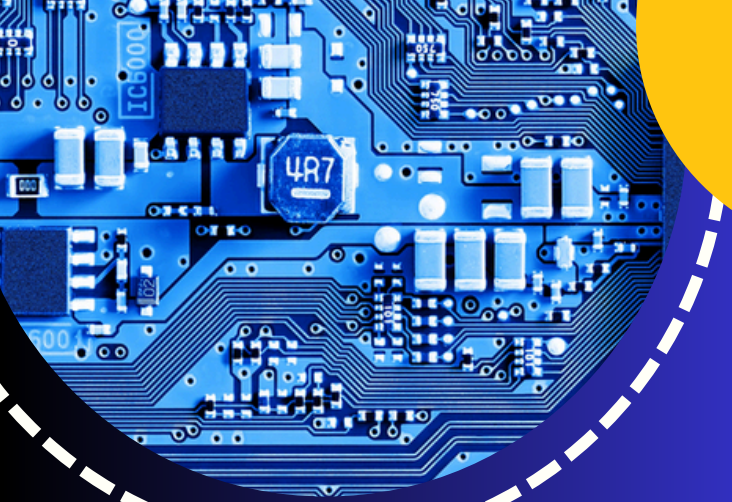


About the Hackathon

In the spirit of India's national chip-design initiatives & under the tech-fest of SGSITS, AAROHAN 2025, the **VLSI Innovators Hackathon** by the Department of Electronics & Instrumentation Engineering, SGSITS, Indore, challenges aspiring engineers to transform ideas into silicon. Participants will push boundaries in Analog and Digital VLSI design—simulating, optimizing, and validating multiple circuit solutions.

Why Participate

Cash Prize
Opportunity to win cash prizes worth Rs. 15,000

Hands-On Learning
Gain practical experience using EDA tools in a simulated environment

Real-World Focus
Tackle authentic design problems inspired by challenges faced in cutting-edge VLSI industries

Comprehensive Skill Development
Delve into crucial aspects of modern VLSI system design.

Hackathon Highlights

Key Dates

2nd Sept 2025 - Registrations open
8th Sept 2025 - Registrations end
19th Sept 2025 - Elimination Round
20th Sept 2025 - Finals

Theme

Analog Design
Digital Design

Support Provided

- EDA software access (e.g., cadence)
- Expert mentorship and debugging support
- Virtual prototyping and simulation infrastructure

Eligibility Criteria

- Open to 2nd, 3rd, and 4th year students of all branches of SGSITS and other institutions.
- Individual participation or a team with a maximum of 2 members allowed.

Guidelines

- Participants must bring their institutional ID card for the hackathon.
- Participants can select only one theme, either analog or digital design.

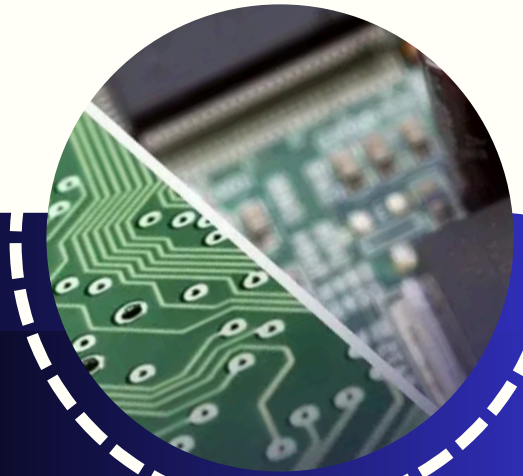
Digital Design (FPGA Based)

Requirements

- RTL code (Verilog or VHDL)
- Testbench and simulation waveforms
- Pin mapping file (fill with your Spartan-7 board's constraints)
- Synthesis report (LUTs, FFs, timing)
- Demo on FPGA board

Problem Statements

- Design and implement a 1-bit half adder and a 1-bit full adder. Extend to a 4-bit ripple carry adder.
- Implement a 4:1 MUX and a 2:4 Decoder.
- Compare two 4-bit numbers and indicate A>B, A==B, A<B
- Design a 4-bit synchronous up counter.
- Implement a finite state machine for two-way traffic control.



Analog Design (ASIC)

Requirements

- Cadence Virtuoso Schematic Editor.
- Use Symbol creation for hierarchy where needed.
- Perform Transient Analysis for waveform verification.
- Document power, area, delay (basic analysis), Transistor count .
- Submit schematics + simulation results + observations.

Problem Statements

- Design, simulate, and verify the working of a D flip-flop using CMOS logic gates in Cadence Virtuoso.
- Create a 4:1 multiplexer circuit using CMOS logic and verify functionality.
- Design an SR flip-flop using CMOS gates.
- Design and simulate a Half Adder using CMOS logic gates in Cadence Virtuoso.
- Design and simulate a Half Subtractor using CMOS logic gates.

Register Now

https://forms.gle/j5m5z8d75QPYeKM77

Scan below to pay the registration fee of Rs.100 per member

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