Shri G. S. Institute of Technology and Science, Indore

Department of Electronics and Instrumentation Engineering

SYLLABUS

M. Tech. (Microelectronics and VLSI Design)

Academic Year 2023-24

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering

Program Outcomes (PO)

For

M. Tech. (Microelectronics and VLSI Design)

PO1: An ability to independently carry out research / investigation and development work to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: Students should be able to demonstrate a degree of mastery over the area as per specialization of program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

PO4: An ability to function effectively as an individual or as a team member in the field of Specialization to achieve the desired objective.

PO5: An ability to engage in independent and life-long learning in the broadest context of technological change.

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering
M. Tech. I Year SEM-I (Microelectronics and VLSI Design)
EI69002: DESIGN OF INTEGRATED CIRCUITS

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
3	-	-	3	-	-	CW	END SEM	SW	END SEM	100
						30	70	-	-	

PRE-REQUISITE: Knowledge of Basic Electronics and Digital Electronics.

COURSE OBJECTIVES:

1. To learn the fundamental principles of CMOS VLSI circuit design in digital domain.
2. To introduce the implementation techniques of logic circuits with CMOS.
3. To introduce the design methodologies for high-speed CMOS and Dynamic logics.

COURSE OUTCOMES: After completion of course, student will be able to:

1. CO1: Classify and explain short channel effects in MOS transistors.
2. CO2: Analyse the CMOS inverter for power and delay trade-offs.
3. CO3: Implement CMOS combinational and Sequential circuits.
4. CO4: Implement and analyse Dynamic CMOS logic & to calculate logical effort.
5. CO5: Design Static RAM and Dynamic RAM cells.

COURSE CONTENTS
THEORY:

UNIT-I Review of MOS transistor theory: Structure and Operation of MOS transistor, threshold voltage, First-order current-voltage characteristics, Short-channel MOS transistor, Deep Submicron Devices (DSM), Short channel effects: Drain punch-through, DIBL, Hot carrier effect, Tunnelling, Velocity saturation. Derivation of velocity saturated Current equation for short channel transistor, Alpha-Power law model, Sub-threshold conduction Body effect, channel length modulation, Capacitances of MOS transistor.

UNIT-II MOS inverter circuits: Introduction, Noise margin definitions, Voltage transfer characteristics (VTC), Calculations of various logic levels (VIL, VOL, VIH, VOH), threshold voltage of Inverter, Resistive load inverter, CMOS inverter, Pseudo-nMOS inverter, Dependence of VTC on W/L ratio, Transistor sizing, Inverter Dynamic characteristics: calculations of tplh and tphl, tr, tf and delay, Power Dissipation in CMOS gates: Static, Dynamic, Power and Delay trade-offs**.**

UNIT-III Static MOS Gate circuits: Introduction, CMOS gate circuits, basic CMOS gate sizing, fan-in and fan-out considerations, VTC of CMOS gates, Complex CMOS gates, XOR and XNOR gates, Multiplier circuits, Flip-flops and Latches, Layout and design criteria, Stick diagrams.

UNIT-IV High-Speed CMOS and Dynamic Logic Design: Switching time analysis, Gate sizing with velocity saturation effect, load capacitance calculations, Gate sizing for optimal path delay, inverter chain optimization, logical effort, optimizing path with logical effort. Dynamic logic design-Pass transistor logic, transmission gate logic, Domino logic, charge sharing, NP Zipper logic etc.

UNIT-V Semiconductor Memory Design: Introduction, Memory organization, types, MOS decoders, Static RAM cell design, DRAM cell design, three-transistor and one transistor dynamic cell Flash memory FRAMS.

ASSESMENT:

Continuous evaluation of students through: Class attendance, Assignments, and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

TEXT BOOKS:

1. Jan M Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits- A Design perspective", Second Edition, PHI, 2003.
2. Sedra and Smith, "Microelectronic Circuits", 5th Edition, Oxford Publications, 2005.
3. S. M. Kang and Y. Leblebici, "CMOS Digital Integrated Circuits", Third Edition, Tata-McGraw Hill, 2003.

REFERENCE BOOKS:

1. David Hodges, Horace Jackson and Rasve Saleh, "Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology", Third Edition, Tata McGraw Hill, 2005
2. Ken Martin, "Digital Integrated Circuit Design", Oxford Publications, 2001.
3. Ming-Bo Lin, "Introduction to VLSI Systems- A Logic, Circuit and System Perspective", CRC Press, 2011.

CO-PO Articulation Matrix

CO-PO	PO1	PO2	PO3	PO4	PO5
CO1	3	2	2	-	-
CO2	3	2	2	-	-
CO3	2	1	1	-	-
CO4	1	1	3	1	1
CO5	1	1	3	1	1
Avg.	2	1.4	2.2	0.4	0.4

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering
M. Tech. I Year I SEM (MICROELECTRONICS & VLSI DESIGN)
EI-69014: HARDWARE DESCRIPTION LANGUAGES

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
3	-	-	3	-	-	30	70	-	-	100

PRE-REQUISITE: Knowledge of Digital Electronics

COURSE OBJECTIVES:

1. To enable the students to design circuits using VHDL and Verilog.
2. Provide the methodology for implementation and simulation of digital circuits.

COURSE OUTCOMES: After completion of course, student will be able to:

1. CO1: Identify the differences between modeling styles of HDL.
2. CO2: Classify Data types, variables, signal, and constants in VHDL.
3. CO3: Design and Simulate VHDL code for combinational and sequential circuits.
4. CO4: Identify arrays, nets, modules and signal assignment statements in Verilog.
5. CO5: Perform the Static Timing Analysis (STA) for digital circuits.

COURSE CONTENTS
THEORY:

UNIT-I: Basic concepts of hardware description languages, Hierarchy, Concurrency, Logic and Delay modelling, Structural, Data-flow and Behavioural styles of hardware description, Architecture of event driven simulators.

UNIT-II: Syntax and Semantics of VHDL, Variable and signal types, arrays and attributes. Operators, expressions and signal assignments, Entities, architecture specification and configurations, Component instantiation.

UNIT-III Concurrent and sequential constructs, Use of Procedures and functions, Examples of design using VHDL.

UNIT-IV: Syntax and Semantics of Verilog, Variable types, arrays and tables. Operators, expressions and signal assignments, Modules, nets and registers.

UNIT-V: Concurrent and sequential constructs, Tasks and functions, Examples of design using Verilog, Synthesis of logic from hardware description, Introduction to System Verilog, Static Timing Analysis (STA).

ASSESMENT:

Continuous evaluation of students through: Class attendance, Assignments, and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

TEXT BOOKS:

1. J. Bhaskar, "VHDL Primer", Pearson Education Asia 2001.
2. Z. Navabi, "VHDL", McGraw Hill International Ed. 1998.
3. S. Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Prentice Hall NJ, USA), 1996.

REFERENCE BOOKS:

1. J. Bhaskar, "Verilog HDL Synthesis - A Practical Primer", Star Galaxy Publishing,(Allentown, PA) 1998.
2. S. Brown and Z. Vranesic, “Fundamentals of Digital Logic with VHDL Design”, Second Edition, McGraw Hill, 2008.
3. D. L. Perry, “VHDL: Programming by Example”, Tata Mc-Graw Hill, 2002.

CO-PO Articulation Matrix

CO-PO	PO1	PO2	PO3	PO4	PO5
CO1	3	2	2	1	1
CO2	3	3	2	1	1
CO3	3	1	1	-	-
CO4	2	2	1	-	-
CO5	2	2	1	-	-
Avg.	2.6	2	1.4	0.4	0.4

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering
M. Tech. I Year I SEM (MICROELECTRONICS & VLSI DESIGN)

EI69005: SEMICONDUCTOR DEVICE AND PROCESS MODELLING

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
3	-	-	3	-	-	CW	END SEM	SW	END SEM	100
						30	70	-	-	

PRE-REQUISITE: Knowledge of Semiconductor & Mathematics.

COURSE OBJECTIVES:

1. To enable the students to understand principles of semiconductor transport.
2. To enable the student to perform analysis of Device structures and behavior.
3. To enable the students to develop their own models for arbitrary device structures.

COURSE OUTCOMES: After completion of course, student will be able to:

1. CO1: Formulate the equations in 1D and 2D for Semiconductor transport.
2. CO2: Develop the modeling equations for diodes, BJT, and MOSFET.
3. CO3: Identify and compute timing and memory requirements for modeling equations.
4. CO4: Model the Semiconductor fabrication processes like diffusion, oxidation etc.
5. CO5: Identify, formulates and solving problems using the techniques and modern programming tools

COURSE CONTENTS

THEORY:

UNIT-I Review of semiconductor theory: Biasing techniques, hybrid model, mathematical modelling of conductivity and resistivity, Poisson's equation, continuity equation, Boltzmann transport equation, diffusion equation\drift, current flow equation, finite difference formulation of these equations in 1D and 2D.

UNIT-II Computation of steady state device characteristic: characteristics of PN junction diode, Exponential diode model, Graphical analysis with Exponential diode model, ideal diode model and real diode model including analysis injection effect, Steady state characteristics of BJT with Eber's moll model and Gummel poon model. Short channel Effects**,** Steady characteristics of MOSFET with charge control model, charge sharing model and channel length modulation, MOS capacitor, small signal steady state analysis and transient analysis, Modelling of Single electron transistor (SET).

UNIT-III Numerical and computational error, computer memory: SRAM, SDRAM, DDR RAM and CPU, Time requirements, efficient linear solvers, Behaviour of Devices, Performance of Devices Circuit simulator: SPICE case study: MINIMOS: Basic features of MINIMOS, MINIMOS6.1, MINIMOS 6.1 WIN, and MINIMOS NT.

UNIT-IV Process Simulation /Process Modelling: Introduction of process simulation, modelling and simulation of oxidation and diffusion, Ion implantation, Masking, Fick's laws, Case Study: SUPERM.

UNIT-V Prerequisite: Familiarity with operation of basic semiconductor devices, Knowledge of one programming language, behaviour of devices, performance of devices, circuit simulator SPICE.

ASSESMENT:

Continuous evaluation of students through: Class attendance, Assignments, and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

TEXT BOOKS:

1. Siegfried Selberherr, "Analysis and Simulation of Semiconductor Devices", Springer Verlag Wien New-York.
2. Walter L. Engl, "Process and Device Modelling", Illustrated Edition, North Holland.
3. R. Raghuram, "Computer Simulation of Electronic Circuits", John Wiley

REFERENCE BOOKS:

1. K. Lee, M. Shur, T.A. Fjedly & T. Yetterdal, "Semiconductor Device Modelling for VLSI, Prentice-Hall.
2. Nandita Dasgupta and Amitava Dasgupta, "Semiconductor Devices: Modelling and Technology", Second Edition, PHI, 2004.
3. Christopher M. Snowden, "Semiconductor Device Modelling", Second Edition, Springer-Verlag, London.

CO-PO Articulation Matrix

CO-PO	PO1	PO2	PO3	PO4	PO5
CO1	3	2	2	1	1
CO2	3	3	2	1	1
CO3	2	3	1	2	2
CO4	2	2	1	-	-
CO5	2	2	1	-	-
Avg.	2.4	2.4	1.4	0.8	0.8

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering
M. Tech. I Year I SEM (MICROELECTRONICS & VLSI DESIGN)
EI69205: ANALOG IC DESIGN
ELECTIVE-I

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
3	-	-	3	-	-	CW	END SEM	SW	END SEM	100
						30	70	-	-	

PRE-REQUISITE: Knowledge of CMOS and analog circuits.

COURSE OBJECTIVES:

1. To prepare the students to gain understanding of CMOS Analog circuits and Systems.
2. To make students familiar with Analog circuit analysis and simulation tool flow.
3. To prepare students to tackle advanced analog IC topics like Op-amp, PLL, ADC, DAC, VCO etc.

COURSE OUTCOMES: After completion of course, student will be able to:

1. **CO1:** Identify and compare the topologies for CMOS amplifier design.
2. **CO2:** Design and Analyze CMSO differential amplifiers with various loads.
3. **CO3:** Design and Analyse various feedback amplifiers.
4. **CO4:** Design CMOS single stage op-amp, two stage op-amp for various performance parameters like slew rate, CMRR, gain, etc.
5. **CO5:** Design CMOS Op-amp comparators, regenerative and high-speed comparators.

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COURSE CONTENTS

THEORY:

UNIT-I Review of MOS devices, Low frequency MOSFET Models, High frequency MOSFET Models, Single-Stage Amplifiers: Basic concepts, common-source stage, common-source stage with resistive load, CS stage with diode-connected load, CS stage with current-source load, CS stage with triode load, CS stage with source degeneration, source follower, common-gate stage, cascade stage, folded cascode, choice of device models.

UNIT-II Differential Amplifiers: Single-ended and differential operation, basic differential pair, qualitative analysis, quantitative analysis, common-mode response, differential pair with MOS loads, gilbert cell.

UNIT-III Frequency Response of Amplifiers: General considerations, Miller effect, association of poles with nodes, common-source stage, source followers, common-gate stage, cascode stage, differential pair. Feedback: General considerations, properties of feedback circuits, types of amplifiers, feedback topologies, voltage-voltage feedback, current-voltage feedback, voltage-current feedback, current-current feedback, effect of loading, two-port network models, loading in voltage-voltage feedback.

UNIT-IV Operational Amplifiers-I: General considerations, performance parameters, one-stage op amps, two-stage op amps, gain boosting, comparison, common-mode feedback, input range limitations, slew rate, power supply rejection. Stability and Frequency Compensation: General considerations, multiple systems, phase margin, frequency compensation, compensation of two stage op amps.

UNIT-V Operational amplifier-II : CMOS Comparator: Characteristic of a comparator, Two stage open loop comparator, Special purpose comparator, Regenerative comparator, High output current amplifier, High speed comparator; Introduction to Switched Capacitor Circuits: Switched capacitor circuits, Switched capacitor amplifiers, Switch capacitor integrators.

ASSESMENT:

Continuous evaluation of students through: Class attendance, Assignments, and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

TEXT BOOKS:

1. B. Razavi, "Design of Analog CMOS Integrated Circuits", Second Edition, McGraw Hill, 2000.
2. Tertulien Ndjountche, "CMOS Analog Integrated Circuits- High Speed and Power Efficient Design", CRS Press.
3. P. R. Gray & R. G. Meyer, "Analysis and Design of Analog Integrated Circuits", 5/e, John Wiley, 2012.

REFERENCE BOOKS:

1. Ken Martin, "Analog Integrated Circuit Design", 2/e, Wiley Publications, 2012.
2. Sedra and Smith, "Microelectronic Circuits", 6/e, Oxford Publications, 2014.
3. Jean-Michel Redoute, Michiel Steyaert, "EMC of Analog Integrated Circuits", Springer, 2010.

CO-PO Articulation Matrix

CO-PO	PO1	PO2	PO3	PO4	PO5
CO1	3	3	2	1	2
CO2	3	3	2	1	2
CO3	2	2	2	-	-
CO4	2	-	-	2	2
CO5	-	-	1	2	2
Avg.	2	1.6	1.4	1.2	1.6

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering
M. Tech. I Year I SEM (MICROELECTRONICS & VLSI DESIGN)

EI 69211: APPLICATION SPECIFIC INTEGRATED CIRCUITS
ELECTIVE-I

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
3	-	-	3	-	-	30	70	-	-	100

PRE-REQUISITE: Studied CMOS Analog and Digital IC Design.

COURSE OBJECTIVES:

1. To prepare students to be entry level industrial standard ASIC/FPCG designer.
2. To give students an understanding of issues and tools related to ASIC design.
3. To give students an understanding of the basics of System on Chip design.

COURSE OUTCOMES: After completion of course, student will be able to:

1. CO1: Demonstrate VLSI tool flow and appropriate FPGA architecture.
2. CO2: Differentiate FPGA architectures of various vendors.
3. CO3: Implement application specific logic circuits with VHDL/Verilog.
4. CO4: Design, simulate, Synthesize, and test state machine-based systems designs.
5. CO5: Formulate testing methodology for ASIC designed.

COURSE CONTENTS

THEORY:

UNIT-I Introduction to ASICs: Types of ASICs, Design Flow, Economics of ASICs, ASIC Cell Libraries, ASIC Library Design: Transistors as Resistors, Transistor Parasitic Capacitance, Logical Effort, Library-Cell Design, Library Architecture, Gate-Array Design, Standard-Cell Design, Data path Cell Design, Programmable ASICs: The Antifuse, Static RAM, EPROM and EEPROM Technology, Practical Issues, Specifications, PREP Benchmarks, FPGA Economics, Programmable ASIC Logic Cells: Actel ACT, Xilinx LCA, Altera FLEX, Altera MA.

UNIT-II Programmable ASIC I/O Cells: DC Output, AC Output, DC Input, AC Input, Clock Input, Power Input, Xilinx I/O Block, Other I/O Cells, Programmable ASIC Interconnect: Actel ACT, Xilinx LCA, Xilinx EPLD, Altera MAX 5000 and 7000, Altera MAX 9000, Altera FLEX, Programmable ASIC Design Software: Design Systems, Logic Synthesis, The Half gate ASIC, Low-Level Design Entry: Schematic Entry, Low-Level Design Languages, PLA Tools, EDIF, CFI Design Representation.

UNIT-III VHDL: A Counter, A 4-bit Multiplier, Syntax and Semantics of VHDL, Identifiers and Literals, Entities and Architectures, Packages and Libraries, Interface Declarations, Type Declarations, Other Declarations, Sequential Statements, Operators, Arithmetic, Concurrent

Statements, Execution, Configurations and Specifications, An Engine Controller, Verilog HDL: A Counter, Basics of the Verilog Language, Operators, Hierarchy, Procedures and Assignments, Timing Controls and Delay, Tasks and Functions, Control Statements, Logic-Gate Modelling, Modelling Delay, Altering Parameters, A Viterbi Decoder, Other Verilog Features.

UNIT-IV Logic Synthesis: A Logic-Synthesis Example, A Comparator/MUX, Inside a Logic Synthesizer, Synthesis of the Viterbi Decoder, Verilog and Logic Synthesis, VHDL and Logic Synthesis, Finite-State Machine Synthesis, Memory Synthesis, The Multiplier, The Engine Controller, Performance-Driven Synthesis, Optimization of the Viterbi Decoder, Simulation: Types of Simulation, The Comparator/MUX Example, Logic Systems, How Logic Simulation Works, Cell Models, Delay Models, Static Timing Analysis, Formal Verification, Switch-Level Simulation, Transistor-Level Simulation.

UNIT-V Test: The Importance of Test, Boundary-Scan Test, Faults, Fault Simulation, Automatic Test Pattern Generation, Scan Test, Built-in Self-test, A Simple Test Example, The Viterbi Decoder Example, Floor planning and Placement: Floor planning, Placement, Physical Design Flow, Information Formats, Routing: Global Routing, Detailed Routing, Special Routing, Circuit Extraction and DRC.

ASSESMENT:

Continuous evaluation of students through: Class attendance, Assignments, and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

TEXT BOOKS:

1. Michael-John Sebastian Smith, "Application-Specific Integrated Circuits, AddisonWesley Publishing Company, VLSI Design Series.
2. H. Gerez, "Algorithms for VLSI Design Automation", John Wiley, 1999.
3. S. Pasricha and N. Dutt, "On-chip Communication Architectures", Elsevier, 2008

REFERENCE BOOKS:

1. Ashok Mehta, "ASIC/SoC Functional Design Verification: A Comprehensive Guide to Technologies and Methodologies", First Edition, Springer, 2018.
2. Razak Hossain, "High Performance ASIC Design- Using Synthesizable Domino Logic in an ASIC Flow", Cambridge University Press, 2009

CO-PO Articulation Matrix

CO-PO	PO1	PO2	PO3	PO4	PO5
CO1	3	3	2	1	1
CO2	3	3	2	1	2
CO3	2	2	2	-	-
CO4	2	-	-	2	2
CO5	3	-	1	2	2
Avg.	2.6	1.6	1.4	1.2	1.4

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering
M. Tech. I Year I SEM (MICROELECTRONICS & VLSI DESIGN)
EI 69206: MEMORY DESIGN AND TESTING
ELECTIVE-I

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
3	-	-	3	-	-					100
						30	70	-	-	

COURSE OBJECTIVES:

1. To acquire knowledge about different types of Semiconductor memories.
2. To give students an understanding of architecture and operation of different types of Semiconductor memories
3. To comprehend the low power design techniques and methodologies.

COURSE OUTCOMES: After completion of course, student will be able to:

1. CO1:Differentiate and Analyze RAM and ROM architectures for performance metrics.
2. CO2:. Design and Analysis of SRAM and DRAM memory cell.
3. CO3: Analyze memory architectures for timing constraints, clock and power gating.
4. CO4: Analysis of different memory testing and Design for Testability (DFT).
5. CO5: Identify new development memory design and testing.

COURSE CONTENTS

THEORY:

UNIT-I: Introduction to Memory Design: Memory hierarchy in computer systems, Classification of memory based on volatility and access types (RAM, ROM, CAM).Memory performance metrics (access time, cycle time, bandwidth, latency),Technology trends and their impact on memory design

UNIT-II: Memory Cell Design and Analysis: Static Random-Access Memory (SRAM): structure, operation, read/write margins, stability analysis, Dynamic Random-Access Memory (DRAM): cell structure, refresh operation, data retention time, soft errors, Content-Addressable Memory (CAM): search operation, design considerations, Memory cell layout and design rules.

UNIT-III: Memory Architecture and Design: Memory organization: bit lines, word lines, sense amplifiers, decoders, Memory array design: addressing schemes, row/column redundancy, hierarchical organization (cache memories). Memory interface design: data paths, control signals, timing constraints, Low-power memory design techniques (clock gating, power gating)

UNIT-IV: Memory Testing and Fault Modelling: Fault models for memory cells (Stuck-at faults, Open/Short faults),Memory testing methodologies: stuck-at fault testing, March tests, memory BIST (Built-In Self-Test), Testing for soft errors and reliability issues, Design-for-testability (DFT) techniques: test points, scan chains, redundancy.

UNIT-V: Advanced Topics in Memory Design & Testing: 3D Stacked Memory: design challenges, thermal considerations, power management, High-Bandwidth Memory (HBM): architecture, interfacing standards.

ASSESMENT:

Continuous evaluation of students through: Class attendance, Assignments, and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

TEXT BOOKS:

1. Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall.
2. Neil H. E. Weste and David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", Fourth Edition, Pearson Education India.
3. Michael L. Bushnell and Vishwani D Agrawal, "Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits", Springer.

REFERENCE BOOKS:

1. R. Dean Adams, "High Performance Memory Testing: Design Principles, Fault Modelling, and Self-Test", Kluwer Academic Publishers, 2002.
2. IEEE International Workshop on Memory Technology, Design, and Testing, IEEE Computer Society, 1997.

CO-PO Articulation Matrix

CO-PO	PO1	PO2	PO3	PO4	PO5
CO1	3	3	3	1	-
CO2	2	3	2	1	-
CO3	3	2	3	2	-
CO4	2	-	-	1	2
CO5	3	-	1	-	2
Avg.	2.6	1.6	1.8	1	0.8

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering
M. Tech. I Year I SEM (MICROELECTRONICS & VLSI DESIGN)
EI69301: VLSI TECHNOLOGY
ELECTIVE-II

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
3	-	-	3	-	-					100
						30	70	-	-	

PRE-REQUISITE: knowledge of basic semiconductors.

COURSE OBJECTIVES:

1. To impart knowledge about the miniaturization of Electronic Systems.
2. To introduce the fundamental concepts relevant to VLSI fabrication.
3. To enable the student to understand the various VLSI fabrication Techniques.

COURSE OUTCOMES: After completion of course, student will be able to:

1. CO1: Identify various design limits materials used for fabrication.
2. CO2: Explain kinetics of oxidation process and its modelling.
3. CO3: Classify lithography techniques and their importance in fabrication.
4. CO4: Model and Characterize diffusion and ion implantation process.
5. CO5: Identify the requirements for clean room during fabrication process.

COURSE CONTENTS

THEORY:

UNIT-I Crystal Growth and Wafer preparation: Wafer terminology, Different crystalline orientations, CZ method, CMOS IC Design flow, Crystal Defects. Fabrication processes of FETs, MOSFETs, and BIMOS etc.

UNIT-II Layering: Epitaxial growth methods; Technological procedures, modelling redistribution of impurities during epitaxy, evaluation of Epitaxial layers, Chemical vapor Deposition, and LPCVD of poly silicon, Oxidation; Kinetics of oxidation, Deal-Grove model and refinements of this model, impurity redistribution during oxidation, ellipsometry. Metallization: Physical Vapor Deposition, Sputtering, Multi-layer interconnects.

UNIT-III Patterning: Lithography; Optical Lithography, Electron Lithography, X-ray Lithography, Ion Lithography. Photo masking steps, Resists, wet and dry etching.

UNIT-IV Doping: Diffusion; Impurity diffusion; solution of diffusion equation, anomalous diffusion and emitter push effect, modeling of diffusion phenomena, Technological processes for diffusion, Characterization of diffused layers, process simulation of Ion Implantation; Implantation Equipment, Principles, techniques and applications, removal of implant damage.

UNIT-V Clean room and safety requirements: Types of clean room, Air Filters, HEPA, ULPA, Clean Air strategy, Contamination source, Total clean room strategy, Micro & Mini Environment, Clean Room Construction and Clean room Layout, wafer cleaning

ASSESMENT:

Continuous evaluation of students through: Class attendance, Assignments, and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

TEXT BOOKS:

1. S.K.Gandhi, "VLSI Fabrication principles", Wiley
2. S.M. Sze, "VLSI Technology", Second Edition, McGraw Hill
3. W.R. Runyan, "Silicon Semiconductor Technology", McGraw Hill.

REFERENCE BOOKS:

1. Y.Chen, "CMOS Devices and Technology for VLSI", Prentice-Hall
2. P.VanZant, "Microchip Fabrication: A Practical Guide to Semiconductor Processing, Third Edition, McGraw Hill.

CO-PO Articulation Matrix

CO-PO	PO1	PO2	PO3	PO4	PO5
CO1	3	3	3	1	-
CO2	2	3	2	1	-
CO3	3	2	3	2	-
CO4	2	-	-	1	2
CO5	3	-	1	-	2
Avg.					

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering
M. Tech. I Year I SEM (MICROELECTRONICS & VLSI DESIGN)

EI69302: MEMS STRUCTURES, SENSORS AND APPLICATIONS
ELECTIVE-II

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
3	-	-	3	-	-	30	70	-	-	100

PRE-REQUISITE: Basic knowledge of Semiconductors, Sensors

COURSE OBJECTIVES:

1. To provide in-depth knowledge of semiconductors and solid mechanics to fabricate MEMS devices.
2. To enable students to learn Micro sensors and Micro actuators.
3. To provide students with in-depth knowledge of MEMS applications in medical, industrial and military fields.

COURSE OUTCOMES: After completion of course, student will be able to:

1. CO1: Identify the materials for MEMS sensors and designing of sensors.
2. CO2: Analyse the basics and scaling laws of micro fabrication methods.
3. CO3: Design Micro actuators for various applications.
4. CO4: Identify the magnetic materials for MEMS magnetic sensing and thermal Sensing.
5. CO5: Apply the concept of MEMS for various applications.

COURSE CONTENTS

THEORY:

UNIT-I: Introduction

Introduction to Micro-Electro-Mechanical Systems (MEMS) Introduction to MEMS and Microsystems, Materials and Substrates for MEMS, Sensors/Transducers, Sensor's characterization and classifications, micro actuators, Application of MEMS.

UNIT-II:Fabrication Technologies

Semiconductor materials, MEMS Fabrication Technologies, single crystal growth, micro-machining, photolithography, microstero lithography, thin film deposition, impurity doping, diffusion, etching, bulk and surface micromaching, etch stop technique and microstructure, LIGA, nanofabrication methods – submicron optical lithography, electron beam lithography.

UNIT-III: Mechanical Sensors & Actuators

Stress and Strain, Hooke's Law, Stress and Strain of Beam Structures, Cantilever, Pressure sensors, Piezo resistance Effect, Piezoelectricity, Piezoresistive Sensor, capacitive sensors,

Inductive sensors, Chemical sensors, MEMS inertial sensors, Parallel-plate Actuator, piezo actuators.

UNIT-IV: Magnetic Sensors and Thermal Sensors

Magnetic material for MEMS, magnetic sensing and detection, magnetoresistive sensors, hall effect, magneto diode, magneto transistors, MEMS magnetic sensors, RF MEMS. Temperature coefficient of resistance, Thermo-electricity, Thermocouples, Thermal and temperature sensors, heat pump, micromachined thermocouple probe, thermal flow sensors, shape memory alloy.

UNIT-V Microfluidics and Applications of MEMS

Scaling laws for microfluidics, transport in micro-channels, microfluidic components e.g. filters, mixers/reactors, valves/controllers, pumps, Applications of MEMS in biomedical field, in military field, in atmospheric measurement and other industrial applications.

ASSESMENT:

Continuous evaluation of students through: Class attendance, Assignments, and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

TEXT BOOKS:

1. James J. Allen, "Micro Electromechanical System Design", Second Edition, CRC Press.
2. Tai Ran Hsu, "MEMS and Microsystem Design and Manufacture", Tata McGraw Hill, 2002.
3. M. J. Usher, "Sensors and Transducers", McMillian Hampshire Publications

REFERENCE BOOKS:

1. Mohamed Gad-El-Hak, "MEMS Design and fabrication", Second Edition, CRC Press.
2. Jan G Korvink, Oliver Paul, "MEMS: A Practical Guide to Design, Analysis and Applications" First Edition, William Andrew Publications.
3. P. Rai Choudhury, "MEMS & MOEMS Technology and Applications", PHI, 2009.

CO-PO Articulation Matrix

CO-PO	PO1	PO2	PO3	PO4	PO5
CO1	3	3	3	1	-
CO2	2	3	2	1	-
CO3	3	2	3	2	-
CO4	2	-	-	1	2
CO5	3	-	1	-	2
Avg.	2.4	1.6	1.8	1	0.8

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering
M. Tech. I Year I SEM (MICROELECTRONICS & VLSI DESIGN)
EI69303: SoC DESIGN
ELECTIVE-II

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
3	-	-	3	-	-	30	70	-	-	100

PRE-REQUISITE: Basic knowledge of Analog and Digital IC design.

COURSE OBJECTIVES:

1. To give the students solid introductory knowledge of System on Chip methodology for logic and analog cores.
2. Understand the performance requirements of complex systems under various operational constraints.
3. Understand different components and design abstractions that contributes towards building complex systems.

COURSE OUTCOMES: After completion of course, student will be able to:

1. CO1: Identify benefits and challenges of SoC design for various applications.
2. CO2: Analyse different SoC architectures and design methodologies
3. CO3: Implement design-for-testability (DFT) strategies for SoCs.
4. CO4: Apply power management concepts to optimize SoC for power.
5. CO5: Design Network-on-Chip architectures for communication in multi-core SoCs.

COURSE CONTENTS

THEORY:

Unit I: Introduction to SoC Design: Evolution of VLSI design: from ASICs to SoCs, Benefits and challenges of SoC design, Applications of SoCs in various domains (mobile devices, automotive, IoT), Classification of SoCs (homogeneous, heterogeneous, multi-core).

Unit II: SoC Architecture and Design Flow: SoC architecture exploration: trade-offs between performance, power, and area, Design flow for SoCs: specification, architectural exploration, functional design, integration, verification, and physical design, Interface design: on-chip communication protocols, bus architectures (AMBA.

Unit III: Hardware Design and Verification for SoCs: Hardware Description Languages (HDLs) for SoC design: Verilog/ System Verilog, Design and modelling of SoC components: processors, memories, peripherals, Design for testability (DFT) techniques for SoCs: scan chains, boundary scan, test wrappers, Formal verification and equivalence checking techniques for SoCs

Unit IV: Power Management and Performance Optimization: Power consumption sources in SoCs: dynamic power, static power, leakage power, Power management techniques for SoCs: clock gating, power gating, voltage scaling, dynamic voltage and frequency scaling (DVFS), Performance optimization strategies for SoCs: pipelining, parallelism, instruction-level parallelism, data-level parallelism

Unit V: Advanced Topics in SoC Design: Network-on-Chip (NoC) architectures for communication in multi-core SoCs, Security considerations in SoC design: hardware security modules, encryption/decryption, Design for reliability techniques for SoCs: fault tolerance, error correction codes, Emerging trends in SoC design: 3D integration, near-threshold computing

ASSESMENT:

Continuous evaluation of students through: Class attendance, Assignments, and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

TEXT BOOKS:

1. Veena S, Chakravarthi, "A Practical approach to VLSI System-on-Chip (SoC) Design", Second Edition, Springer, 2020.
2. Michael J Flynn and Wayne Luk, "Computer System Design: System-on-Chip", Wiley, 2011.
3. Douglas Smith, "HDL Chip Design: A Practical Guide for Designing, Synthesizing and Simulating ASICs and FPGAs Using VHDL or Verilog", Doone Pubns Publications.

REFERENCE BOOKS:

1. Bashir M. Al-Hashimi, "System on Chip-Next Generation Electronics", Institution of Engineering and Technology (IET), 2006.
2. Li-Shiuan Peh and Natalie Enright Jerger, "On-Chip Networks", First Edition, Morgan and Clypool Publications.
3. Youn-Long Steve Lin, "Essentials issues in SoC Design: Designing Complex Systems-on-Chip", Springer Verlag.

CO-PO Articulation Matrix

CO-PO	PO1	PO2	PO3	PO4	PO5
CO1	2	3	2	1	1
CO2	2	2	3	1	-
CO3	1	2	3	-	-
CO4	2	3	-	2	2
CO5	3	2	1	1	2
Avg.	2	2.4	1.6	1	1

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering
M. Tech. I Year SEM-II (Microelectronics and VLSI Design)
EI69451: LAB-I: CAD TOOL DESIGN LAB-1

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
-	4	-	-	2	-	-	-	40	60	100

PRE-REQUISITE: Knowledge of Linux and CMOS circuit design.

LABORATORY OBJECTIVES:

1. Demonstrate the ability to use Mentor-Graphics EDA tools for CMOS circuit design.
2. Explore the schematic design aspects of CMOS combinational and sequential circuits.
3. Explore layout design aspects of CMOS combinational and sequential circuits.

LABORATORY OUTCOMES: On completion of lab course, the student will be able to:

1. CO1:Able to use the Mentor-Graphics EDA tools for ASIC Design flow.
2. CO2: Design CMOS logic circuits using Mentor Graphics and Tanner Tool.
3. CO3: Able to use Eldo simulator to analyze functional and timings of logic circuits.
4. CO4: Design the layout of CMOS circuits using Pyxis tool.
5. CO5: Demonstrate the use of Caliber tool for physical verification of layout.

LIST OF EXPRIMENTS:

1. Introduction to EDA tools design flow (Mentor Graphics/ Tanner).
2. To simulate the VI characteristics of NMOS and PMOS to obtain various performance parameters.
3. To obtain voltage transfer characteristics of CMOS inverter and observe the effect to varying W/L ratio on VTC.
4. To obtain the dynamic characteristics of CMOS inverter.
5. To design and verify performance parameters of 2 input NAND & NOR gates based on inverter sizing.
6. To implement two input NAND & NOR gates using domino logic and compare its performance with CMOS logic.
7. To implement and simulate 4-bit full adder using CMOS transistors.
8. Study the various design rules for layout using 180 nm technology.
9. Design the layout of CMOS inverter using 180nm technology & observe the effect of parasitics on its performance.
10. Design the Layout of 4-bit Full adder using 180 nm technology.

ASSESMENT:
Continuous evaluation of students through: Lab attendance, Lab Journals and performance, and internal viva with weightage of 40% of total marks. End semester practical exam. Weightage is 60% of total marks.

CO-PO Articulation Matrix

CO-PO	PO1	PO2	PO3	PO4	PO5
CO1	2	3	2	1	1
CO2	2	2	3	1	-
CO3	3	2	3	-	-
CO4	3	-	-	1	2
CO5	-	2	1	-	2
Avg.	2	1.8	1.8	0.6	0.6

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering
M. Tech. I Year SEM-II (Microelectronics and VLSI Design)
EI69452: CAD TOOL DESIGN LAB-II

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
-	4	-	-	2	-	-	-	40	60	100

PRE-REQUISITE: Basic of Digital electronics & familiarity with syntax of VHDL

LABORATORY OBJECTIVES:

1. To learn Hardware Descriptive Language (VHDL/Verilog).
2. To learn the simulation of VHDL/Verilog code using Modelsim.
3. To learn how to use FPGA devices to download VHDL code to verify functionality.

LABORATORY OUTCOMES: On completion of lab course, the student will be able to:

1. CO1**:** Write VHDL code using Xilinx Tool.
2. CO2: Model digital systems in VHDL at different levels of abstraction.
3. CO3: Demonstrate different design styles to simulate various logic circuits.
4. CO4: Demonstrate the use of Xilinx synthesis tool to generate netlist for hardware.
5. CO5: Demonstrate use of FPGA boards with Xilinx to download VHDL code.

LIST OF EXPRIMENTS:

Combination Circuit Design Exercise

1. Write and simulate the VHDL code for logic Gates.
2. Design and Simulate Half adder and Full adder using VHDL.
3. Design, Simulate, and Synthesize Half Subtractor and full Subtractor using VHDL.
4. Design and simulate 2*4 and 3*8 Decoders with various modeling techniques using VHDL.
5. Design and simulate 8*3 Encoder using different modeling techniques using VHDL.
6. Design, simulate and synthesize 4*1 multiplexer using various concurrent and sequential statements using VHDL.
7. Design, simulate, Synthesize and download 8*3 Encoder using VHDL on Spartan FPGA Board.
8. Implement and simulate various flip flops using (If-then-else) Sequential constructs.
9. Design, Simulate, and Synthesize 8bit Synchronous Johnson counter.
10. Design, Simulate, Synthesize and Download MOD-16 up counter on Spartan FPGA boards.

ASSESMENT:

Continuous evaluation of students through: Lab attendance, Lab Journals and performance, and internal viva with weightage of 40% of total marks. End semester practical exam. Weightage is 60% of total marks.

CO-PO Articulation Matrix

CO-PO	PO1	PO2	PO3	PO4	PO5
CO1	2	3	2	1	1
CO2	2	2	3	1	-
CO3	3	2	3	-	-
CO4	3	-	-	1	2
CO5	-	2	1	-	2
Avg.	2	1.8	1.8	0.6	1

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering
M. Tech. I Year SEM-II (Microelectronics and VLSI Design)
EI69501: COMMUNICATION RF IC DESIGN

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
3	-	-	3	-	-	CW	END SEM	SW	END SEM	100
						30	70	-	-	

PRE-REQUISITE: Knowledge of Signals & Systems, Basic Communication, Analog IC Design.

COURSE OBJECTIVES:
The objective of this course is to present the concept of design and analysis of modern RF and wireless communication integrated circuits.

COURSE OUTCOMES: After completion of course, student will be able to:
1. **CO1:** Apply transmission line theory and S-parameters at high frequency.
2. **CO2:** Identify the specifications of RF systems.
3. **CO3:** Classify and differentiate the trans-receiver architectures.
4. **CO4:** Apply RF concepts to design LNA and Mixer.
5. **CO5:** Apply RF concepts to design VCO, PLL and layout at high RF.

COURSE CONTENTS

THEORY:

UNIT-I
Review of RF Theory: RF range, skin effect, behaviour of various passive components like R, L, C, at high RF, their equivalent circuits at high RF. Transmission line theory, reflection coefficient, Smith chart calculation, impedance matching, S-parameter.

UNIT-II
Basic concepts in RF design: RF dc design. Hexagon wireless communication standards, nonlinearity, harmonics, gain compression, desensitization, cross modulation, inter modulation distortion (IMD), input intercept point (IIP3 & IIP2), inter symbol interference, Noise, types of noise, noise analysis of active devices.

UNIT-III
Trans-receiver Architecture: TRF receivers, heterodyne receivers, Homodyne receivers, their comparison, type RF receiver architecture and its design

UNIT-IV

Design concepts-1: Low noise amplifiers, Noise Reduction techniques, various topologies, comparison and design, Mixers, Linearity improvement techniques, various topologies, comparison and design, Filters- type and design.

UNIT-V

Design Concepts-2: VCO, PLL, various types, comparison and design. Frequency synthesizes and their design IC application and case studies for DECT, GSM and Bluetooth. Layout issues in RF IC design,

ASSESMENT:

Continuous evaluation of students through: Class attendance, Assignments, and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

TEXT BOOKS:

1. BehzadRazavi, "RF Microelectronics", Second edition, Prentice Hall,1998
2. Thomas H. Lee, "The design of CMOS radio frequency integrated circuits", Second Edition, Cambridge University Press.
3. R. Ludwig and P. Bretcheko, "RF Circuit Design", Second Edition, Pearson.

REFERENCE BOOKS:

1. L. E. Larson, "RF and Microwave circuit design for wireless communication", Artech House Publication 1997.
2. Robert H. Caverly, "CMOS RFIC Design Principles", Artech House Publications.

CO-PO Articulation Matrix

CO-PO	PO1	PO2	PO3	PO4	PO5
CO1	3	3	2	-	-
CO2	3	3	2	-	-
CO3	2	2	2	1	1
CO4	1	1	3	2	2
CO5	1	1	3	2	2
Avg.	2	2	2.6	1	1

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering
M. Tech. I Year SEM-II (Microelectronics and VLSI Design)
EI69502: MIXED SIGNAL CIRCUIT DESIGN

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
3	-	-	3	-	-	30	70	-	-	100

PRE-REQUISITE: Knowledge of designing Analog and Digital Circuits.

COURSE OBJECTIVES:

1. Learn how to design and analyze mixed signal integrated circuits.
2. Learn how to design Analog-to-Digital converters and Digital-to-Analog converters.
3. Learn how to model delays and interconnects in VLSI circuits.

COURSE OUTCOMES: After completion of course, student will be able to:

1. **CO1:** Design the Bi-CMOS circuits for desired noise margin and power dissipation.
2. **CO2:** Analyse analog and digital sub circuits like current sink, source and voltage references.
3. **CO3:** Differentiate between current mode and voltage mode signal processing.
4. **CO4:** Classify, Differentiate, and design various ADC and DACs.
5. **CO5:** Model the interconnects and delays with CAD tools.

COURSE CONTENTS

THEORY:

UNIT-I

BiCMOS devices and technology: BiCMOS inverter and logic gates, Characteristics, Noise Margin and Power dissipation, BiCMOS operational Amplifier, Comparison of BiCMOS, Bipolar and CMOS technology.

UNIT-II

Basic Analog and Digital sub circuit: Switches, Active resistors, Current sinks and sources, Current mirrors, current and voltage references, Band gap reference, Power dissipation and noise analysis.

UNIT-III

Current mode signal processing: Current conveyor, current mode differentiator, Integrator, summer, Advantage of current mode circuits, Current normalizer, current correlator and Bump circuit.

UNIT-IV

Continuous time and sampled data signal processor, Current scaling D/A, voltage scaling, charge scaling D/A, Nyquist rate ADC, Pipeline ADC, Interpolating ADC, Folding ADC, Over Sampled ADC, Delta Sigma ADC, ADC & DAC characteristics, and parameters.

UNIT-V

Analog VLSI Interconnects: Physics and Scaling of interconnects logic and interconnect design, delay modelling, wire sizing, buffer insertion, cross talk minimization, resistive, capacitive, and inductive interconnects.

Statistical modelling of devices and circuits: Computer Aided analog design, CAD system, T-SPICE, Analog and Mixed (Analog and digital) circuit layouts.

ASSESMENT:

Continuous evaluation of students through: Class attendance, Assignments, and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

TEXT BOOKS:

1. Randall L. Geiger, Philip E. Allen, Noel R Strades, "VLSI Design techniques for Analogand Digital Circuits", Second edition, McGraw Hills Publications.
2. David Johns, Ken Martin, "Analog Integrated Circuit Design", Second edition, John Wiley Publications.
3. Philip E Allen, Douglas R Holberg, "CMOS Analog Circuit Design", Oxford publications

REFERENCE BOOKS:

1. Jacob Baker, Harry W.Li, David E. Boyce, "CMOS Circuit Design Layout and Simulation",Prentice Hall.
2. Jacob Baker, "CMOS Mixed Signal Circuit Design", IEEE Press, 2009.
3. Gregorian, Temes, "Analog MOS Integrated Circuits for Signal Processing", John Wiley & Sons, 1986.

CO-PO Articulation Matrix

CO-PO	PO1	PO2	PO3	PO4	PO5
CO1	2	2	2	2	2
CO2	2	3	2	1	1
CO3	2	2	2	2	2
CO4	3	2	1	-	-
CO5	3	2	1	2	2
Avg.	2.4	2.2	1.6	1.4	1.4

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering
M. Tech. I Year SEM-II (Microelectronics and VLSI Design)
EI69503: VLSI TEST AND TESTABILITY

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
3	-	-	3	-	-	CW	END SEM	SW	END SEM	100
						30	70	-	-	

PRE-REQUISITE: Knowledge of Digital Integrated Circuits

COURSE OBJECTIVES:

1. To involve the students in theory and practice of VLSI test and validation.
2. To introduce advanced techniques for efficiently testing and validating VLSI design.
3. To introduce the concept of Design for Test and the technique for automated test pattern generation.

COURSE OUTCOMES: Upon successful completion of this course, student will be able to:

1. **CO1:** Identify the challenges in VLSI testing and differentiate approaches for testing.
2. **CO2:** Detect and model the fault in VLSI circuits and simulate it.
3. **CO3:** Define the methodology to test combinational and sequential circuits.
4. **CO4:** Apply concept of BIST and IDQQ for testing memory and other VLSI circuits.
5. **CO5:** To construct a Design for Testability (DFT) algorithm for VLSI circuits.

COURSE CONTENTS

THEORY:

UNIT-I

Fabrication Assembly and Test Process: Introduction to testing process, types of testing at IC level, IC production test process, Burn-in-Board, system and field testing, cost of testing, Importance of testing, Challenges in VLSI testing, Levels of abstractions in VLSI testing, Functional vs. Structural approach to testing, Complexity of the testing problem, Relations and functions, Boolean function representation canonicity and equivalence Boolean satisfiability.

UNIT-II

Fault Modelling and Simulation: Circuit modelling, Introduction to fault, fault detection and redundancy, fault equivalence and fault dominance, Stuck at fault, bridging faults, transistor faults, delay faults etc. fault collapsing and fault sampling simulation, simulation techniques, compiled simulation, event-driven simulation, series, parallel deductive and concurrent fault simulation.

UNIT-III

Test generation for combination and sequential circuits: D-algorithm, PODEM, Boolean satisfiability, automatic test pattern generation, primitive and propagation cubes, path

oriented decision making, fan-out oriented test generation, DFT for combinational and sequential digital circuits. LSSD techniques

UNIT-IV

Built in self-test and IDDQ testing: RAM BIST, logic BIST, BIST pattern generation and response analyzer, scan-based BITS architecture, random and weighted random pattern testability, test point insertion for improving random testability, Fundamental of IDDQ testability, IDDQ testing The LFSRs and their use in random test generation and response compression

UNIT-V

Design for testability: Controllability & observability, Models of sequential circuits, state table method self-initializing test sequences, undetectability, distinguishing and synchronizing sequences, and complexity of sequential ATGP, Built in self-test for VLSI chips.

ASSESMENT:

Continuous evaluation of students through: Class attendance, Assignments, and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

TEXT BOOKS:

1. Parag K Lala, "Self-checking and fault tolerance Digital Design", First edition Academic Press.
2. Viswani D. Agrawal, Micheal L Bushnell, "Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits", Kluwer Academic Publications, 2000.
3. P. K. Lala, **"**Digital Circuit Testing and Testability", Academic press.

REFERENCE BOOKS:

1. M. Abramovici, M.A. Brever, A.D. Friedman, "Digital System Testing and Testable Design, IEEE Press.
2. Alfred L. Crouch, "Design for Test for Digital ICs and Embedded Core Systems", Prentice Hall, 1999.
3. Kanad Chakraborty and Pinaki Mazumdar, Fault Tolerance and Reliability Techniques for High-Density Random-Access Memories, Prentice Hall.

CO-PO Articulation Matrix

CO-PO	PO1	PO2	PO3	PO4	PO5
CO1	3	2	2	2	2
CO2	3	2	2	2	2
CO3	3	3	2	-	-
CO4	2	2	1	-	-
CO5	2	1	1	1	1
Avg.	2.6	2	1.6	1	1

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering
M. Tech. I Year SEM-II (Microelectronics and VLSI Design)
EI69705: SYSTEM HARDWARE DESIGN (Elective-III)

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
3	-	-	3	-	-	30	70	-	-	100

PRE-REQUISITE: Knowledge of basic Digital Electronics, CMOS Design

COURSE OBJECTIVES:

1. Enable the students to apply their knowledge for the design of advanced digital hardware systems with the help of FPGA.
2. Learn how to implement power distribution and clocking strategies and clock distribution.
3. Learn how to design noise tolerant systems.

COURSE OUTCOMES: Upon successful completion of this course, student will be able to:

1. **CO1:** Design advanced digital logic with optimized power, timing and ESD issues.
2. **CO2:** Analyse the clock distribution and system timings for digital systems.
3. **CO3:** Design Synchronous and Asynchronous circuits and multilayer PCB design.
4. **CO4:** Design Noise tolerant digital systems and apply EMI concepts to digital systems.
5. **CO5:** Design real time systems with FPGA/CPLD.

COURSE CONTENTS

THEORY:

UNIT-I

Advance digital logic design: Sequential, Combinational and State Machines, Design issues based on power dissipation, timing and loading and case studies, CMOS, BICMOS and TTL noise and ESD issues.

UNIT-II

Basic System Design aspect: Power distribution, Clocking strategies, Clocked system, Latch and Resistors, System timing, two phase clocking, four phase clocking, Clock distributions, Signal connection and Signal quality.

UNIT-III

Synchronous and Asynchronous design and multilayer PCB design. Interface between devices, boards and units.

UNIT-IV

Transient switching problems and worst-case timing. Timing analysis and optimization Noise tolerant design, EMI related design aspects, Noise in MOS transistors and resistors, Noise examples.

UNIT-V

Memory based subsystem design, Static RAM, Dynamic Ram, Field programmable gate array (FPGA), CPLD based design. Microcontroller (8 bit and 16 bit) and their applications, Analog design issues some examples of real-life system.

ASSESMENT:

Continuous evaluation of students through: Class attendance, Assignments, and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

TEXT BOOKS:

1. Wayne Wolf, "Modern VLSI Design: System on chip design", Second edition, Pearson Education.
2. Randall L. Geiger, Philip E. Allen, Noel R Strades, "VLSI Design techniques for Analog and Digital Circuits", Second edition, McGraw Hills Publications.
3. Wayne Wolf, "FPGA Based System Design", Prentice Hall

REFERENCE BOOKS:

1. Krzysztof Iniewski, "Embedded Systems: Hardware, Design, and Implementation", Second Edition, Wiley.
2. Philip E Allen, Douglas R Holberg, "CMOS Analog Circuit Design", Oxford publications

CO-PO Articulation Matrix

CO-PO	PO1	PO2	PO3	PO4	PO5
CO1	3	2	2	1	1
CO2	3	2	2	1	1
CO3	3	3	2	-	-
CO4	2	2	1	-	-
CO5	2	1	1	1	1
Avg.					

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering
M. Tech. I Year SEM-II (Microelectronics and VLSI Design)
EI69706: EMBEDDED SYSTEM DESIGN (Elective – III)

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
3	-	-	3	-	-	30	70	-	-	100

PRE-REQUISITE: Knowledge of programming languages and operating systems.

COURSE OBJECTIVES:

1. To make the students learn the fundamental principles of embedded system design.
2. Develop embedded system software using assembly language and C programming.
3. Utilize real-time operating systems (RTOS) for task management and resource allocation.

COURSE OUTCOMES: After completion of course, student will be able to:

1. **CO1:** Identify the applications of embedded systems in various domains.
2. **CO2:** Classify and explain the architectures of embedded processors.
3. **CO3:** Write the assembly language program for embedded systems.
4. **CO4:** Apply concept of real time operating system (RTOS) in embedded systems
5. **CO5:** Optimize and test the embedded system for performance parameters.

COURSE CONTENTS

THEORY:

Unit 1: Introduction to Embedded Systems: Definition and characteristics of embedded systems, Applications of embedded systems in various domains (IoT, automotive, consumer electronics), Hardware components of an embedded system (processor, memory, peripherals), Design challenges and trade-offs in embedded systems (performance, power, cost, size), Hardware-software co-design methodologies for embedded systems.

Unit 2: Embedded System Architectures: Embedded processor architectures (ARM, MIPS, RISC-V), Memory hierarchies in embedded systems (cache, main memory), Interfacing peripherals: buses, communication protocols (SPI, I2C), Interrupt service routines (ISRs) for handling hardware events, Input/Output (I/O) programming and device drivers

Unit 3: Embedded System Programming: Assembly language programming for embedded systems: instruction sets, addressing modes, C programming for embedded systems: memory management, pointer arithmetic, bit manipulation, Real-time programming concepts: scheduling, concurrency, tasks, semaphores Interfacing hardware from software: memory-mapped I/O, device drivers

Unit 4: Real-Time Operating Systems (RTOS): Introduction to Real-Time Operating Systems (RTOS) for embedded systems, Task management and scheduling in RTOS:

priorities, pre-emptive vs. non-preemptive, Inter-process communication (IPC) mechanisms: semaphores, message queues, Memory management in RTOS: static vs. dynamic allocation, Popular RTOS for embedded systems (Free RTOS, Wind River etc.)

Unit 5: Design Optimization and Testing: Design optimization for embedded systems: performance, power consumption, resource utilization, Low-power design techniques for embedded systems, Testing methodologies for embedded systems: unit testing, integration testing, system testing, Embedded system debugging tools and techniques.

ASSESMENT:
Continuous evaluation of students through: Class attendance, Assignments, and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

TEXT BOOKS:

1. David E. Simon, "Embedded Systems Design: A Unified Hardware/Software Introduction", 3rd edition, John Wiley
2. Raj Kamal, "Embedded Systems: Architecture, Programming and Design", Second edition, Tata McGraw Hill.

REFERENCE BOOKS:

1. Jonathan W. Valvano, "Embedded Microcomputer Systems: Real Time Interfacing", 3rd edition, Thomson.
2. David Barr, "The Embedded Real-Time Operating System", 2nd edition, PHI

CO-PO Articulation Matrix

CO-PO	PO1	PO2	PO3	PO4	PO5
CO1	3	2	2	1	1
CO2	3	2	2	1	1
CO3	3	3	2	-	-
CO4	2	2	1	-	-
CO5	2	1	1	1	1
Avg.					

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering
M. Tech. I Year SEM-II (Microelectronics and VLSI Design)
EI69707: VLSI SIGNAL PROCESSING (Elective – III)

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
3	-	-	3	-	-	30	70	-	-	100

PRE-REQUISITE: Knowledge of Signal Processing, HDL

COURSE OBJECTIVES: This course will introduce approaches and methodologies for VLSI design of signal processing.

1. To introduce techniques for altering the existing DSP architectures to suit VLSI implementation.
2. To introduce efficient design of DSP architectures suitable for VLSI.

COURSE OUTCOMES: After completion of course, student will be able to:

1. **CO1:** Identify the applications of VLSI DSP systems.
2. **CO2:** Implement the algorithms for basic DSP operations.
3. **CO3:** Optimization of DSP processors for performance using HDL-Verilog/ System Verilog.
4. **CO4:** Apply concept of clock and power gating to design low power DSP processors.
5. **CO5:** Apply concept of Hardware accelerators for specific DSP applications.

COURSE CONTENTS

THEORY:

Unit 1: Introduction to VLSI Signal Processing: Review of digital signal processing (DSP) fundamentals (sampling, quantization, filtering),Challenges and opportunities in VLSI DSP design, Applications of VLSI DSP systems (audio/video processing, communication systems, image processing)

Unit 2: DSP Algorithm Architectures: Architectures for basic DSP operations: adders, multipliers, accumulators, Pipelined and parallel architectures for high-performance DSP, Systolic arrays for efficient implementation of specific algorithms, Hardware architectures for common DSP algorithms (FIR filters, IIR filters, FFT), Finite word length effects and quantization noise in VLSI DSP

Unit 3: Design Techniques and Optimization: Hardware Description Languages (HDLs) for VLSI DSP design: Verilog / System Verilog, Pipelining and parallelism techniques for performance optimization, Area optimization techniques: bit-width optimization, resource sharing

Unit 4: Low-Power VLSI Signal Processing: Low-power design techniques for VLSI DSP circuits: clock gating, power gating, Voltage Scaling, Low power signal processing architectures, Trade-offs between speed and power

Unit 5: Advanced Topics in VLSI Signal Processing: VLSI architectures for high-performance computing: DSP cores, multi-core processors, Hardware accelerators for specific DSP applications, Reconfigurable computing for VLSI DSP: FPGAs.

ASSESMENT:
Continuous evaluation of students through: Class attendance, Assignments, and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

TEXT BOOKS:

1. Richard G. Lyons, "Understanding Digital Signal Processing"
2. Keshab K. Parhi, "VLSI Digital Signal Processing Systems: Design and Implementation", Wiley Interscience, 2007
3. Mohammad Ismail, Terri Fiez, “Analog Signal and VLSI Processing”, McGraw Hill 1993.

REFERENCE BOOKS:

1. U Meyer Baese, "Digital Signal Processing with field Programmable Gate Arrays", Second edition, Springer, 2004
2. Kung S. Y., H. J. White House, T. Kailath, "VLSI and Modern Signal Processing”, 2nd edition, Prentice Hall, 1985.

CO-PO Articulation Matrix

CO-PO	PO1	PO2	PO3	PO4	PO5
CO1	3	2	2	2	2
CO2	2	3	2	-	-
CO3	3	3	2	-	-
CO4	2	2	1	2	2
CO5	2	1	1	1	1
Avg.	2.4	2.2	1.6	1	1

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering
M. Tech. I Year SEM-II (Microelectronics and VLSI Design)
EI69751: LOW POWER VLSI DESIGN (Elective-IV)

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
3	-	-	3	-	-	30	70	-	-	100

PRE-REQUISITE: Knowledge of CMOS VLSI design.

COURSE OBJECTIVES:

1. To expose the students to the low voltage device modeling, low voltage and low power CMOS circuit design.
2. To introduce various software power estimation and optimization techniques for low power VLSI system design

COURSE OUTCOMES: After completion of course, student will be able to:

1. CO1**:** Justify the need for low power-VLSI circuits.
2. CO2: Analyse the transistor and gate sizing, pin ordering for low voltage, low power design.
3. CO3: Discuss Power reduction in clock networks- CMOS floating node- low power bus- delay balancing- SRAM.
4. CO4: Implement the algorithm for analysis and optimization of low power circuits.
5. CO5: Discuss low power circuit design styles.

COURSE CONTENTS

THEORY:

UNIT-I: Introduction to low power VLSI design-Need for low power-CMOS leakage current-static current-Basic principles of low power design-probabilistic power analysis random logic signal-probability and frequency-power analysis techniques-signal entropy.

UNIT-II: Circuit- transistor and gate sizing- pin ordering- network reconstructing and reorganization-adjustable threshold voltages-logic-signal gating-logic encoding. Precomputation logic.

UNIT-III: Power reduction in clock networks- CMOS floating node- low power bus- delay balancing- SRAM, Switching activity reduction, parallel voltage reduction, operator reduction- Adiabatic computation- pass transistor logic.

UNIT-IV: Algorithm and architectural level methodologies- Introduction, design flow, algorithmic level analysis and optimization, architectural level estimation and synthesis.

UNIT-V: Low power circuit design style- Software power estimation –co design.

ASSESMENT:

Continuous evaluation of students through: Class attendance, Assignments, and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

TEXT BOOKS:

1. Gary Yeap, "Practical Low Power Digital VLSI Design", McGraw Hill, 1997.
2. Kaushik Roy, Sharat C. Prasad, "Low Power CMOS VLSI circuit design", Wiley Interscience Publications, 1987.

REFERENCE BOOKS:

1. Rabey, Pedram, "Low power design methodologies" Kluwer Academics, 1997.
2. Anantha P. Chandrakasan & Robert W. Brodersen, "Low Power Digital CMOS Design", Kluwer Academics Publications, 1994.
3. A. Bellameur & M.J. Elmauri, "Low Power VLSI CMOS circuit design", Kluwer Academics Press, 1995.

CO-PO Articulation Matrix

CO-PO	PO1	PO2	PO3	PO4	PO5
CO1	3	2	2	1	1
CO2	3	2	2	1	1
CO3	2	3	3	-	-
CO4	2	2	1	-	-
CO5	2	2	1	1	1
Avg.	2.4	2.2	1.8	0.6	0.6

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering
M. Tech. I Year SEM-II (Microelectronics and VLSI Design)
EI69752: NANO TECHNOLOGY (Elective-IV)

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
3	-	-	3	-	-	30	70	-	-	100

PRE-REQUISITE: Basics of Semiconductor materials and Physics.

COURSE OBJECTIVES:

1. To achieve an understanding of the theory of quantum mechanics.
2. To develop an ability to apply quantum theory to important physical systems.
3. To acquire the knowledge of basic sciences required to understand the fundamentals of nanomaterials.

COURSE OUTCOMES: After completion of course, student will be able to:

1. CO1: List the techniques of synthesis of nano-materials and application of nano-materials.
2. CO2: Correlate the physical behaviour of materials at the nanoscale with quantum mechanics.
3. CO3: List the mechanical and thermal properties of Nanomaterials.
4. CO4: Identify the nanostructure and behaviour of particle at nano level.
5. CO5: Apply the knowledge gained to suggest different applications nanotechnology.

COURSE CONTENTS

THEORY:

UNIT-I

Introduction of nanomaterials and nanotechnologies, Features of nanostructures, Background of nanostructures, Techniques of synthesis of nanomaterials, Tools of the nanoscience, Applications of nanomaterials and technologies

UNIT-II

Introduction to Quantum Mechanics; Schrodinger equation and expectation values, Solutions of the Schrodinger equation for free particle, particle in a box, particle in a finite well, Reflection and transmission by a potential step and by a rectangular barrier.

UNIT-III

Bonding and structure of the nanomaterials, Predicting the Type of Bonding in a Substance crystal structure, Metallic nanoparticles, Surfaces of Materials, Nanoparticle Size and Properties, Mechanical properties of materials, theories relevant to mechanical properties, techniques to study mechanical properties of nanomaterials, adhesion and friction, thermal properties of nanomaterials.

UNIT-IV

Confinement and Transport in nanostructure, Current, Reservoirs and Electron channels, Conductance formula for nanostructures, Quantized conductance, Local density of states. Ballistic transport, Coulomb blockade, Diffusive transport, Fock space.

UNIT-V

Nano thin films, nano composites, new application of nanoparticles in different fields, Carbon Nanotubes Types of nanotubes and their formation, Properties of nanotubes, Uses in nanoelectronics, Carbon nanotube transistors, Quantum computer, Spintronics, Molecular electronic devices, Future prospects.

ASSESMENT:

Continuous evaluation of students through: Class attendance, Assignments, and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

TEXT BOOKS:

1. B. H. Bransden and C. J. Joachain, "Quantum Mechanics", Second Edition, Pearson, 2000.
2. Mark Ratner and Daniel Ratner, "Nanotechnology: A Gentle Introduction to Next Big Idea", First Edition, Pearson, 2002.
3. Richard D. Booker and Earl Boysen, "Nanotechnology for Dummies", John Wiley & Sons, 2005.

REFERENCE BOOKS:

1. Stuart Lindsay, "Introduction to Nanoscience" OUP Oxford,2009.
2. Thomas Varghese, "Nanotechnology: An Introduction to Synthesis Properties and Applications of Nanomaterials", first Edition Atlantic Publications, 2023.
3. B. Bhushan, "Handbook of Nanotechnology", Second Edition, Springer, 2007.

CO-PO Articulation Matrix

CO-PO	PO1	PO2	PO3	PO4	PO5
CO1	3	2	2	2	1
CO2	3	3	2	2	1
CO3	2	3	3	1	1
CO4	2	2	1	-	-
CO5	2	1	1	1	1
Avg.	2.4	2.2	1.8	1.2	0.8

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering
M. Tech. I Year SEM-II (Microelectronics and VLSI Design)
EI69753: OPTOELECTRONIC INTEGRATED CIRCUIT
(Elective-IV)

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
3	-	-	3	-	-	CW	END SEM	SW	END SEM	100
						30	70	-	-	

PRE-REQUISITE: Knowledge of Optical Communication

COURSE OBJECTIVES:

1. To provide the students with an understanding of various semiconductors and non-semiconductor-based optoelectronics devices.
2. To impart the knowledge on optical waveguide fabrication and characterization.
3. To make students aware of the latest technology used in optical integrated circuits.

COURSE OUTCOMES: After completion of course, student will be able to:

CO1: Explain principle of Optical Waveguide, its equations**.**
CO2: Illustrate optical waveguide fabrication and characterization.
CO3: Explain use of optical coupling, switching and optical modulator.
CO4: Identify different detectors and their use in optical communications.
CO5: Analyze the latest development in Optical Integrated circuits.

COURSE CONTENTS

THEORY:

UNIT-I

Theory of Optical Waveguides: Waveguide theory: one dimensional planar waveguide, two-dimension waveguide, transcendental equations, waveguide modes, cutoff conditions.

UNIT-II

Optical waveguide fabrication and characterization: waveguide fabrication: Deposited films; vacuum deposition and solution deposition, diffused waveguides, ion exchange and ion implanted waveguides, Epitaxial growth of III-V compound semiconductor materials, shaping of waveguides by wet and dry etching techniques. Waveguide characterization: surface scattering and absorption losses, radiation and bending losses, measurement of waveguides loss, waveguides profiling.

UNIT-III

Fundamental of optical coupling: Transverse coupler, prism coupler, grating coupler, fiber to waveguide coupler, coupling between optical waveguides, directional coupler, Application of directional coupler.

UNIT-IV

Guided wave modulators and switches: Physical effect used in light modulators: electro-optic, acousto-optic, and magneto-optic effects, Waveguide modulators and switches. Semiconductor laser and detectors: laser diode, distributed feedback lasers, integrated optical detectors.

UNIT-V

Recent progress in integrated optics: state-of-the-art technology in guided wave devices and application, in e.g. photonic switching, tunable laser diodes, optical integrated circuits.

ASSESMENT:

Continuous evaluation of students through: Class attendance, Assignments, and two mid Semester Tests Exam with weightage of 30% of total marks. End semester theory exam. Weightage is 70% of total marks.

TEXT BOOKS:

1. Behzad Razavi, "Design of Integrated Circuits for Optical Communication", Second Edition, Wiley and Sons Ltd., 2012.
2. Horst Zimmermann, "Silicon Optoelectronic Integrated Circuits", Springer, 2018.
3. R. Sysm and J. Cozens, "Optical Guided Waves and Devices", McGraw Hill, 1993.

REFERENCE BOOKS:

1. Hiroshi Nishihara, Masamitsu Haruna and Toshiaki Suhara, "Optical Integrated Circuits", McGraw Hill, 2002.
2. Edmond J. Murphy(ed), "Integrated Optical Circuits and Components: Design and Applications", World Scientific Publishing Ltd. U. S. A. 2020

CO-PO Articulation Matrix

CO-PO	PO1	PO2	PO3	PO4	PO5
CO1	3	2	2	1	1
CO2	3	2	2	1	1
CO3	3	3	2	-	-
CO4	2	2	1	-	-
CO5	2	1	1	1	1
Avg.	2.6	2	1.6	0.6	0.6

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering
M. Tech. I Year SEM-II (Microelectronics and VLSI Design)
EI69851: LAB-III: VLSI Design Lab-1

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
-	4	-	-	2	-	-	-	40	60	100

PRE-REQUISITE: Basic Linux. Analog-Digital Integrated Circuits, RFIC design.

LABORATORY OBJECTIVES:

1. Demonstrate the ability to use Cadence EDA tool for CMOS circuit design.
2. Students will be given hands-on of Virtuoso schematic and layout of CMOS circuits.
3. Students will be provided with a hands-on Spectre simulator for simulation and Assura for physical verification (DRC, LVS, and RCX) of CMOS circuits.

LABORATORY OUTCOMES: On completion of lab course, the student will be able to:

1. CO1: Able to use the Cadence EDA tools for CMOS circuits design.
2. CO2: Design CMOS logic circuits using Virtuoso Schematic editor of Cadence.
3. CO3: Able to use Spectre simulator to analyze functional and timings of logic circuits.
4. CO4: Design the layout of CMOS circuits using Virtuoso layout editor tool.
5. CO5: Demonstrate the use of Assura tool for physical verification of layout.

LIST OF EXPRIMENTS:

1. Introduction to Cadence EDA tools design flow.
2. Design CMOS inverter and simulate its voltage transfer characteristics using Spectre simulator and observe the effect to varying W/L ratio on VTC.
3. Implement two input NAND & NOR gates in Virtuoso Schematic editor and perform Transient and DC analysis based on inverter sizing.
4. Implement full adder using Virtuoso Schematic editor, simulate it with Spectre simulator, draw its layout using Virtuoso layout editor. Perform physical verification with Assura (drc, lvs, rcx) tool.
5. Design CMOS OP-AMP and perform its transient, dc and ac analysis to obtain the performance parameters like, gain, CMRR, Slew rate.
6. Design a CMOS Low Noise Amplifier (LNA) and perform its Noise and Scattering (S-parameter) analysis to obtain performance parameters like Noise, S11, S12, S21 and S22.
7. Design Voltage-Controlled Oscillator (VCO) and perform analysis to obtain its phase noise.
8. Starting from Specification design 4-bit adder using SCL 180nm technology and obtain its GDSII file to be sent for tape out.

ASSESMENT:

Continuous evaluation of students through: Lab attendance, Lab Journals and performance, and internal viva with weightage of 40% of total marks. End semester practical exam. Weightage is 60% of total marks.

CO-PO Articulation Matrix

CO-PO	PO1	PO2	PO3	PO4	PO5
CO1	2	3	2	1	1
CO2	2	2	3	1	-
CO3	3	2	3	-	-
CO4	3	-	-	1	2
CO5	-	2	1	-	2
Avg.	2	1.8	1.8	0.6	1

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering
M. Tech. I Year SEM-II (Microelectronics and VLSI Design)
EI69852: LAB-IV: VLSI Design Lab-2

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
-	4	-	-	2	-	-	-	40	60	100

PRE-REQUISITE: Basic Linux, Analog and Digital integrated circuits.

LABORATORY OBJECTIVES:

1. To train the students in RTL-to-GDSII flow using Mentor-Graphics EDA tool.
2. To give students hands-on experience on complete chip design flow.

LABORATORY OUTCOMES: On completion of lab course, the student will be able to:

1. CO1: Perform Front End to Back End Design Flow with the help of Mentor Graphics.
2. CO2: Demonstrate the use of HDL Designer to write VHDL/Verilog code of digital ckt.
3. CO3: Use Precision Synthesis RTL, Leonardo Spectrum to synthesize the design.
4. CO4: Use Calibre to perform DRC, LVS, RCX and post layout simulation.
5. CO5: Demonstrate the complete chip design flow from RTL-to-GDSII.

LIST OF EXPRIMENTS:

1. Implement the synchronous counter to learn the Design Flow of HDL Designer.
2. To implement full adder using VHDL in HDL Designer.
3. To implement mod 8 up counter using state diagram entry method in Mentor Graphics Tool.
4. To implement Johnson counter using block diagram entry method in Mentor Graphics Tool.
5. To implement multiplexer by using Truth Table Entry Method in Mentor Graphics Tool.
6. To implement a 8*8 Rom using Truth Table Entry Method in Mentor Graphics Tool.
7. To study Semi-Custom-Back End-Flow using Mentor Graphics Tool.
8. To implement a 8 bit ALU from Specifications-to RTL-to GDSII with the help of Mentor Graphics Tool.

ASSESMENT:

Continuous evaluation of students through: Lab attendance, Lab Journals and performance, and internal viva with weightage of 40% of total marks. End semester practical exam. Weightage is 60% of total marks.

CO-PO Articulation Matrix

CO-PO	PO1	PO2	PO3	PO4	PO5
CO1	2	3	2	1	1
CO2	2	2	3	1	-
CO3	3	2	3	-	-
CO4	3	-	-	1	2
CO5	-	2	1	-	2
Avg.					

Shri G. S. Institute of Technology and Science, Indore
Department of Electronics and Instrumentation Engineering
M. Tech. II Year SEM-III (Microelectronics and VLSI Design)
EI69931: SEMINAR

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
-	8	-	4	-	-	-	-	50	-	50

COURSE OUTCOMES: Students will be able to:

1. CO1: Demonstrate a sound technical knowledge of their selected seminar topics.
2. CO2: Identify the problem, its formulation and provide techniques for its solution.
3. CO3: Design engineering solutions to complex problems utilizing system approach.
4. CO4: Develop communication skills with engineers and community at large.

CRITERIA & RUBRICS:

Maximum Marks: 50 Marks

Student will be judged using following criteria and rubrics:

1. Technical Content- 10 Marks (CO1, CO2, CO3, CO4)
2. Presentation Capabilities- 10 Marks (CO1, CO2, CO3, CO4)
3. Knowledge -10 (CO1, CO2, CO3, CO4)
4. Documentation – 10 (CO1, CO2, CO3, CO4)
5. Confidence- 10 (CO1, CO2, CO3, CO4)

Shri G. S. Institute of Technology and Science
Department of Electronics and Instrumentation Engineering
M. Tech. II Year SEM-III (Microelectronics and VLSI Design)

MA85902/**69902**/75902/84902/51902/52902/59902/54902/71902/87902/8902/65902/61902/63902

RESEARCH METHODOLOGY & IPR

HOURS PER WEEK			CREDITS			MAX. MARKS				
T	P	TU	T	P	TU	THEORY		PRACTICAL		TOTAL MARKS
						CW	END SEM	SW	END SEM	
2	-	-	2	-	-	30	70	-	-	100

COURSE OBJECTIVE

1. Discuss the research types, methodology and formulation.
2. Identify the sources of literature, survey, review and quality journals.
3. Discuss the research design for collection of research data.
4. Analyze the research data and write the research report.
5. To identify and apply appropriate research methodology in order to plan, conduct and evaluate basic research.

COURSE OUTCOMES: The students will be able to

1. CO#1 Illustrate the research types and methodology.
2. CO#2 Collect research data and use various tools and techniques for data analysis
3. CO#3 Do literature survey using quality journals.
4. CO#4 Process research data to write research report for grant proposal.
5. CO#5 Understanding the importance and benefit of IPR protection.

COURSE CONTENTS

THEORY

Unit 1: Research: Types of research, research process, research proposals and aspects, research methodology, objectives of research, motivation in research, significance of research, selecting the research problem, scope and objective of research problem, Technique involved in defining a problem.

Unit 2: Statistical Tools: Measures of central tendency, measures of dispersion and measures of relationship: correlation and regression analysis. Data Sampling, Testing & Research

Modeling: Student T-test, F-test, analysis of variance (ANOVA), data graphics and data interpretation.

Unit 3: Literature Review: National and international scenario of scientific research. effective literature reviewing, reference citation, scientific, engineering and research journals, impact valuation, indexing and abstracting.

Unit 4: Report Writing: Significance of report writing, types, formats, steps of report writing and publications in research journals, Technique of interpretation, and presentation, Plagiarism and research ethics.

Unit 5: Patents, Designs, Trademarks, Geographical Indications and Copyright, Process of patenting and development, international cooperation on Intellectual Property, Scope of patent rights, Licensing and transfer of technology Patent information and databases, new developments in IPR.

ASSESSMENT

1. Internal Assessment for continuous evaluation, mid-term tests, assignments, seminars, class performance, etc. (30%).
2. End semester Theory Exam (70%).

TEXT BOOKS RECOMMENDED

1. C.R Kothari, "Research Methodology, Methods & Technique", New Age International Publishers, New Delhi, 2004.
2. R. P. Merges, P. S. Menell, M.A. Lemley, "Intellectual Property in New Technological Age", 2016.

REFERENCE BOOKS:

1. R. Ganesan, "Research Methodology for Engineers", MJP Publishers, Chennai, 2011.
2. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008