



4 WEEK INTERNSHIP ON

CHIP DESIGN FLOW USING CADENCE

CONTENT

- **Introduction to Basic Flow of Cadence Tool.**
- **Introduction to Basic CMOS Circuit Design.**
- **Simulation Of Schematic Design.**
- **Layout Design Rules.**
- **RC Extraction Flow.**
- **Post Layout Simulation.**
- **Work On CMOS Based Project.**

Shri G.S. Institute Of Technology & Science, Indore



Department Of Electronics & Instrumentation Engg.

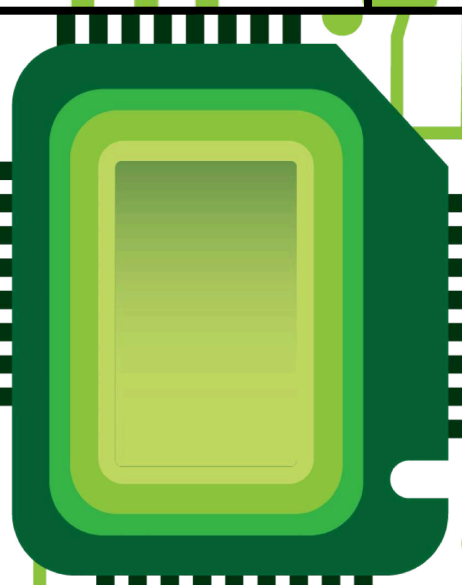
4 WEEK INTERNSHIP ON

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Schedule

WEEK 1 and WEEK 2

DAYS	10:30 AM - 11:30 AM	11:30 AM - 12:30 PM	12:30 PM - 01:30 PM	01:30 PM - 05:30 PM
MONDAY TO SATURDAY	Dr. RAJESH KHATRI	Dr. R.C. GURJAR	LUNCH BREAK	LAB SESSION



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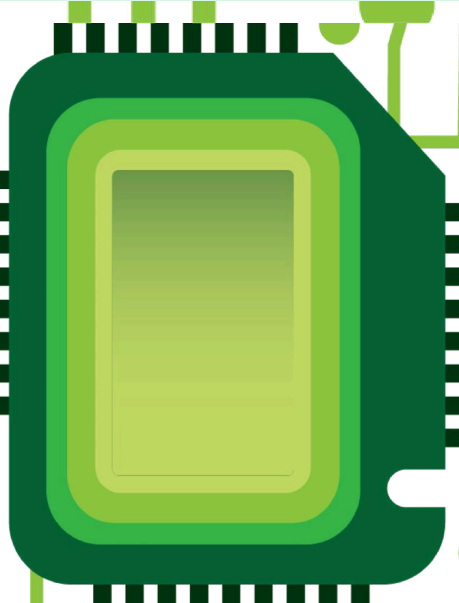
4 WEEK INTERNSHIP ON

CHIP DESIGN FLOW USING CADENCE

Schedule

WEEK 3 and WEEK 4

DAYS	10:30 AM - 01:00 PM	01:00 PM - 02:00 PM	02:00 PM - 05:00 PM
MONDAY TO SATURDAY	LAB SESSION (Project)	LUNCH BREAK	LAB SESSION (Project)



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4 WEEK INTERNSHIP ON *CHIP DESIGN FLOW USING CADENCE*

Lab Session 1st week - Hands On Practice

1. Cadence tool flow.
2. Schematic Simulation.
3. Ac, Dc, Transient Analysis.

Lab Session 2nd week - Hands On Practice

1. Layout Using Virtuoso Tool.
2. DRC, LVS, RCX with Assura Tool.
3. Post Layout Simulation
4. GDS-II file Generation

